Electromagnetic Compatibility Principles and Design

(Schneider Electric, April 1-3, 2025)

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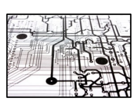
Agenda (Day 1)

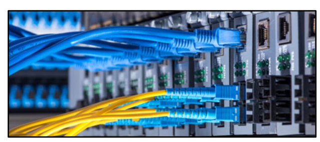
1. Introduction
- Overview of Electromagnetic Compatibility
- Coupling Mechanisms
- Analog, Digital and Power Circuits

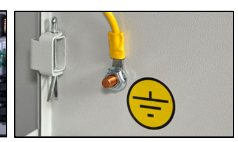
2. Circuit Components and Parasitics
- Resistance, Capacitance and Inductance
- Absolute, Self, and Mutual Capacitance
- Self, Mutual and Partial Inductance
- Component Parasitics
- Estimating Parasitic Values



3. Signal Routing and Termination
- Tracing Current Paths / Concept of Least Impedance
- Transition Time Control
- RLC Circuits
- Transmission Lines

4. Identifying the Unintentional Antennas
- Essential Elements of an Antenna
- What Makes a Good Antenna
- What Makes a Poor Antenna





5. Noise Sources and Coupling Mechanisms
- Integrated Circuits as Sources of EMI
- Parasitic Oscillations and Unexpected Noise Sources
- Coupling Between Noise Sources and Antennas
- Differential Mode to Common Mode Conversion

6. Grounding
- Definition of Ground
- EMC Ground vs. Current Return
- EMC Ground vs. Safety Ground
- Ground Structures and Grounding Conductors

7. "Ground" in Mixed-Signal Environments
- Analog and Digital Components on a PCB
- Power Ground
- Ground in Circuit Simulations

Agenda (Day 2)

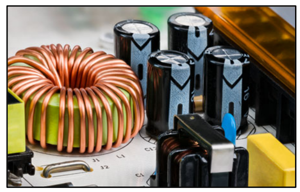
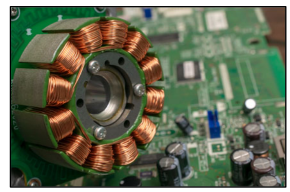
8. Filtering
- Insertion Loss
- First-Order Low-Pass Filters
- Second-Order Low-Pass Filters
- Component Parasitics

9. Transient Protection
- TVS Diodes and MOVs
- Thyristors and GDTs
- When to Use It
- How to Connect It

10. Shielding
- Electric Field Shielding
- Magnetic Field Shielding
- Shielding Enclosures
- Cable Shielding

11. DC Power Distribution and Decoupling
- Effective Power Distribution Strategies
- Choosing and Locating Decoupling Capacitors
- Low-Inductance Capacitor Connections
- Isolating PLLs and Other Sensitive Devices

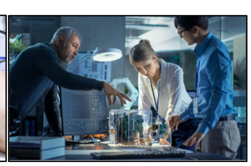
12. Power Electronics Design for EMC
- Board Layout of Power Electronics Circuits
- Filtering to Control Conducted Emissions
- Component Selection and Placement

Agenda (Day 3)

13. Key System-Level Design Considerations
- For Conducted Emissions Tests
- For Radiated Emissions Tests
- For Radiated Immunity Tests
- For Electrical Fast Transient Tests
- For Lightning Surge Tests
- For Electrostatic Discharge Tests

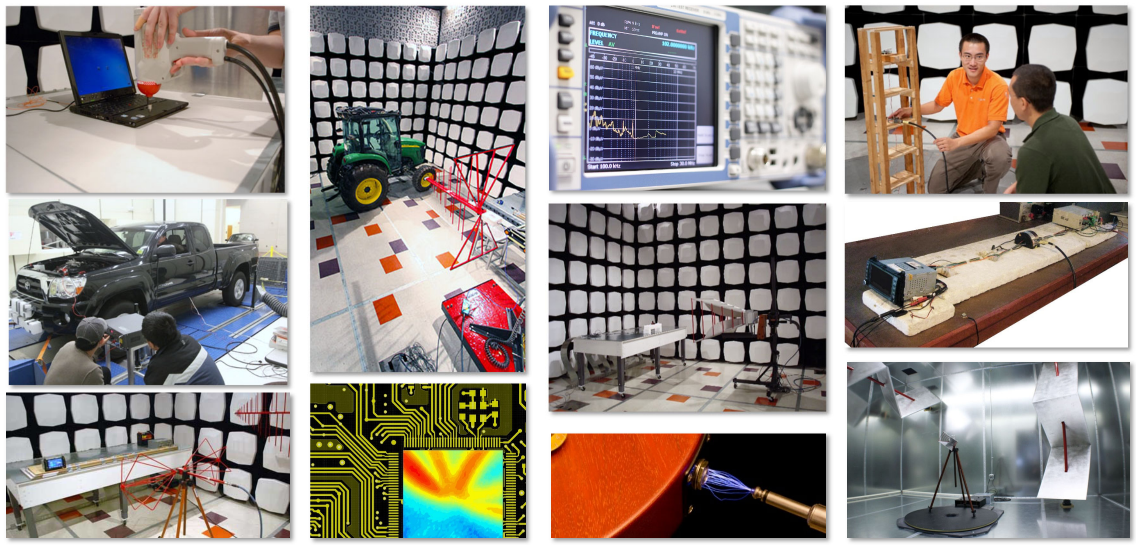
14. An EMC Compliance Strategy
- Reviewing a Circuit Board Design
- Reviewing a System Design
- Identifying Grounds, Current Paths and Antennas
- Recognizing Safety Critical EMC Issues
- Performing a Worst-Case Analysis

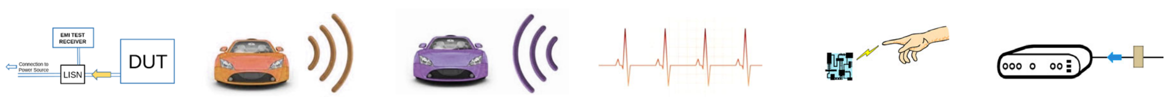

15. Specific Design Examples
- Circuit Breaker
- Ethernet Interface
- Examples Provided by the Class

16. Course Summary
- Review of Key Concepts
- Resources for EMC Problem Solving

Electromagnetic Compatibility Measurements



EMC Requirements and Key Design Considerations



Conducted Emissions
- 1 HF GND
- SMPS Layout
- Filter Design
- Filter Layout
- Balance Control
- Transition Times
- Decoupling

Radiated Emissions
- 1 HF GND
- PCB Layout
- Risetime Control
- Filtered I/O
- Decoupling
- Balance Control

Radiated Immunity
- 1 HF GND
- Filtered I/O
- Transition Times
- Victim ID
- Decoupling
- Balance Control

Transient Immunity
- PCB GND
- Filtered I/O
- Transient Protection
- Victim ID
- Bandwidth Control

Electrostatic Discharge
- Arc Management
- PCB GND
- Bandwidth Control
- LF Current Path
- HF Current Path
- Filtered I/O
- Transient Protection

Bulk Current Injection
- 1 HF GND
- HF Current Path
- Chassis GND
- Filtered I/O
- Identify Key Circuits
- Bandwidth Control

Designing a product that is guaranteed to meet all these requirements is relatively straight-forward.
Fixing a non-compliant product can be difficult and costly.

Question for ChatGPT

How should I layout my printed circuit board to meet electromagnetic compatibility requirements?

Designing a printed circuit board (PCB) to meet electromagnetic compatibility (EMC) requirements involves careful consideration of several key factors. Here are some essential guidelines to help you layout your PCB for optimal EMC performance:

1. Signal Integrity

- **Trace Routing:** Keep signal traces as short and direct as possible to reduce inductance and resistance. **Use wider traces** or planes for high-current paths to minimize voltage drops and electromagnetic interference (EMI).
- **Ground Planes:** Implement solid ground planes to provide a low-impedance return path for sign [illegible] in reducing EMI and maintaining signal integrity. A solid ground plane also aids in minimizing crosstalk between traces.
- **Signal Traces:** Route high-speed and high-frequency signals as short as [illegible] ce by adhering to trace width and spacing guidelines. **Use differential pairs for high-speed signals**, if app [illegible]

2. Power Integrity

- **Decoupling Capacitors:** Place deco [illegible] ency noise. **Use a combination of capacitor values** (e.g., 0.1 μF, 1 μF) for effecti [illegible]
- **Power and Ground Pla** [illegible] **and ground** to minimize noise coupling. Ensure that power planes are adequately bypassed and that they have sufficient [illegible]

BAD ADVICE!

3. EMI Reduction

- **Shielding:** Incorporate shielding techniques such as metal enclosures or PCB shielding layers to block EMI from sensitive components. **Design your PCB layout to minimize the gaps and seams in shields.**
- **Component Placement:** Place sensitive components away from high-noise sources like switching regulators and high-speed digital circuits. **Isolate high-frequency components** to reduce their impact on analog or low-speed circuits.
- **Layer Stack-Up:** Utilize a proper layer stack-up to improve EMC performance. Typically, a stack-up with **alternating signal and ground planes** helps in controlling impedance and reducing EMI.

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Question for ChatGPT

4. Trace Routing and Layout

- **Avoid Loops:** Minimize loop areas in signal and power traces. **Large loop areas can act as antennas and radiate EMI.**
- **Use Short Return Paths:** Ensure that the **return path for a signal is as short as possible**, ideally beneath the signal trace on the same layer or on an adjacent ground plane.
- **Grounding**: Use multiple ground vias to connect ground planes across different layers and reduc [illegible] pedance. **Implement a star grounding approach** if applicable.

5. Board Edge Considerations

- **Edge Traces:** Avoid routing high-speed or sensitive traces n [illegible] the edge, **add an edge connector or grounding** to minimize emissions.
- **Edge Connector Grounding:** Ens [illegible] to prevent EMI and maintain signal integrity.

BAD ADVICE!

6. Testing and Validatio [illegible]

- **Simulations:** Use sin [illegible] **performance of your PCB.** Simulate signal integrity, power integrity, and EMC to predict and address potential issues befor [illegible]
- **Prototyping and Testi** [illegible] prototypes and conduct EMC testing (such as radiated and conducted emissions tests) to identify and resolve issues. **Make iterative design improvements based on test results.**

7. Compliance with Standards

- **Standards:** Familiarize yourself with relevant EMC standards and guidelines (e.g., IEC 61000, FCC Part 15). Ensure that your design meets these standards to pass regulatory testing and certification.

By following these guidelines and continuously refining your design based on testing and simulations, you can effectively manage electromagnetic compatibility and ensure reliable PCB performance.

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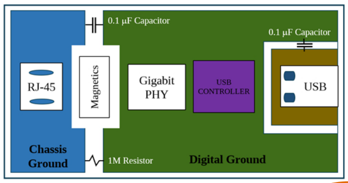
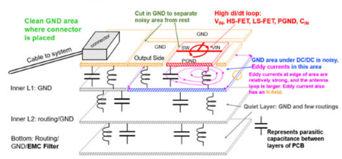
Learn to Recognize Design Errors that Result in EM Interference

Bad Layout Advice



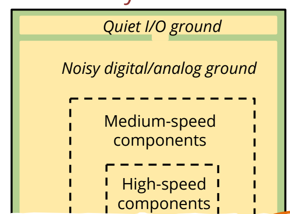
2023

Bad Stackup Advice



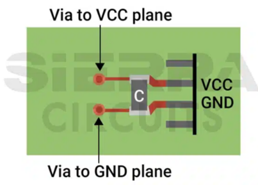
2023

Bad Layout Advice



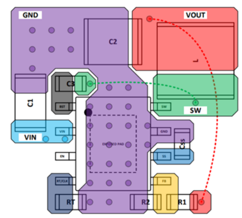
2023

Bad Decoupling Advice



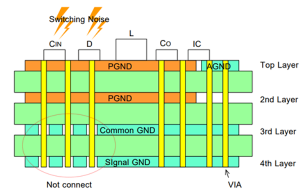
2025

Bad Layout Advice



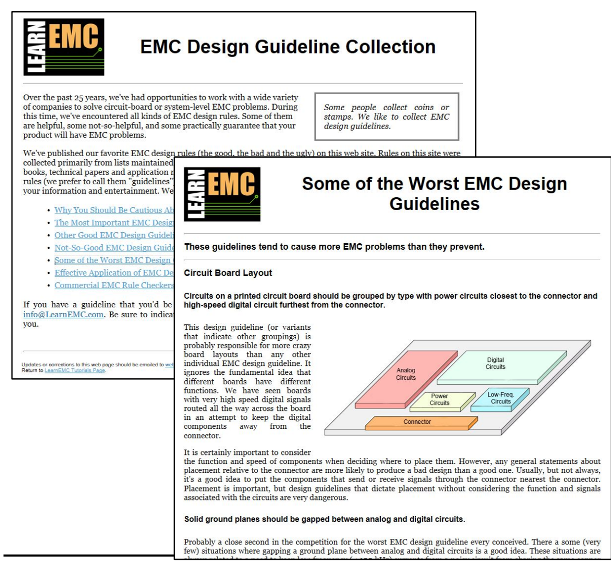
2024

Bad Converter Stackup



2024

EMC Design Rules/Guidelines



EMC Design Guideline Collection

Over the past 25 years, we've had opportunities to work with a wide variety of companies to solve circuit-board or system-level EMC problems. During this time, we've encountered all kinds of EMC design rules. Some of them are helpful, some not-so-helpful, and some practically guarantee that your product will have EMC problems.

Some people collect coins or stamps. We like to collect EMC design guidelines.

We've published our favorite EMC design rules (the good, the bad and the ugly) on this web site. Rules on this site were collected primarily from lists maintained ... books, technical papers and application ... rules (we prefer to call them "guidelines" ... your information and entertainment. We ...

- Why You Should Be Cautious Ab...
- The Most Important EMC Desig...
- Other Good EMC Design Guideli...
- Not-So-Good EMC Design Guide...
- Some of the Worst EMC Design ...
- Effective Application of EMC De...
- Commercial EMC Rule Checkers...

If you have a guideline that you'd be ... info@LearnEMC.com. Be sure to indica... you.

Some of the Worst EMC Design Guidelines

These guidelines tend to cause more EMC problems than they prevent.

Circuit Board Layout

Circuits on a printed circuit board should be grouped by type with power circuits closest to the connector and high-speed digital circuit furthest from the connector.

This design guideline (or variants that indicate other groupings) is probably responsible for more crazy board layouts than any other individual EMC design guideline. It ignores the fundamental idea that different boards have different functions. We have seen boards with very high speed digital signals routed all the way across the board in an attempt to keep the digital components away from the connector.

Analog Circuits
Digital Circuits
Power Circuits
Low-Freq. Circuits
Connector

It is certainly important to consider the function and speed of components when deciding where to place them. However, any general statements about placement relative to the connector are more likely to produce a bad design than a good one. Usually, but not always, it's a good idea to put the components that send or receive signals through the connector nearest the connector. Placement is important, but design guidelines that dictate placement without considering the function and signals associated with the circuits are very dangerous.

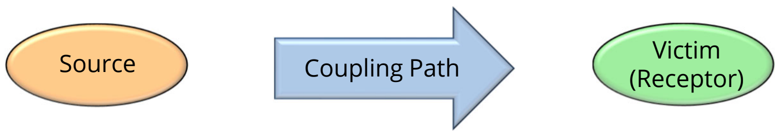
Solid ground planes should be gapped between analog and digital circuits.

Probably a close second in the competition for the worst EMC design guideline every conceived. There a some (very few) situations where gapping a ground plane between analog and digital circuits is a good idea. These situations are

- Rules that work well in some designs can be completely inappropriate for other designs.
- Many rules widely published in books, app notes, and data sheets are NEVER appropriate.
- Complying with a long list of EMC design rules is a terrible way to do a board layout.

Essential Elements of an EMC Problem

All EMC problems have a source, coupling path and victim.



Lightning	Cables	Integrated Circuit
RF Transmitter	Antennas	RF Receiver
High Speed Data Trace	Common Ground	High Speed Data Trace
Electric Motor	Power Lines	Cell Phone
Arc Welder	Parasitic Capacitance	Electronic Controls
Video Display	Parasitic Inductance	Video Display

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Coupling Paths

There are only 4 possible coupling mechanisms!

- Conducted Coupling
- Electric Field Coupling
- Magnetic Field Coupling
- Radiation Coupling

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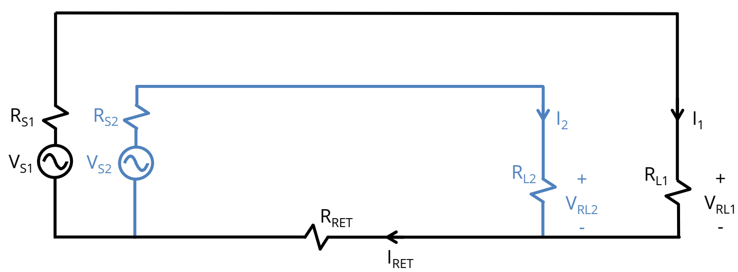
Conducted Coupling

aka: Common Impedance Coupling



- Requires 2 conductor connections between the source and victim.
- The only mechanism that couples DC level shifts.
- Most likely to be dominant at low frequencies, when source and victim share a current return path.
- Most likely to be dominant when sources are low impedance (high current) circuits.

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Conducted Coupling

Examples

- Lights dim and radio dies when automobile engine is started
- Power bus voltage spikes are heard as audible “clicks” on an AM radio using the same power source
- An electrostatic discharge transient damages a system component
- A lightning induced transient destroys the electronic components in an ECU

Solutions

- Eliminate common impedance by routing return currents independently
- Reduce common impedance by using a lower impedance source or return path
- Isolate signals in frequency by filtering
- Isolate signals in time

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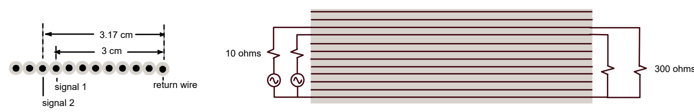
Basic Calculations

Common Impedance Coupling in a Ribbon Cable

A 10-ohm function generator sends a 1-volt, 3.0-MHz sine wave to a 300-ohm load through a 0.75-meter ribbon cable. The return wire (ground) is 3.0 cm away from the signal wire in the same ribbon cable. The radius of each wire in the ribbon cable is 0.32 mm. Another wire in the same cable is located 0.17 cm away from the first signal wire. This wire is also attached to a 10-ohm source and a 300-ohm load and uses the same return (ground) wire as the first circuit. Calculate the coupled voltage and amount of crosstalk (in dB) due to common impedance coupling between the two circuits.



$$\delta_{cu@3MHz} = \frac{1}{\sqrt{\pi f \mu \sigma_{cu}}} = \frac{1}{\sqrt{\pi\left(3\times10^{6}\ \text{Hz}\right)\left(4\pi\times10^{-7}\ \text{H/m}\right)\left(5.8\times10^{7}\ \text{S/m}\right)}} = 38.2\times10^{-6}\ \text{m}$$

$$R_{wire} = \frac{l}{\sigma_{cu} 2\pi a\delta} = \frac{0.75\ \text{m}}{\left(5.8\times10^{7}\ \text{S/m}\right)2\pi\left(3.2\times10^{-4}\ \text{m}\right)\left(38.2\times10^{-6}\ \text{m}\right)} = 0.169\ \Omega$$

$$V_{RL2} = I_{RET}R_{RET}\left(\frac{300}{300+10}\right) = \frac{V_{RL1}}{300}\left(0.169\ \Omega\right)\left(\frac{300}{300+10}\right) = 5.44\times10^{-4}V_{RL1}$$

$$\text{Xtalk}_{21} = 20\log\left|\frac{V_{RL2}}{V_{RL1}}\right| = 20\log\left|5.44\times10^{-4}\right| = -65\text{dB}$$

$$V_{RL2} = 5.44\times10^{-4}\ V_{RL1} = 5.44\times10^{-4}\ \text{V}$$

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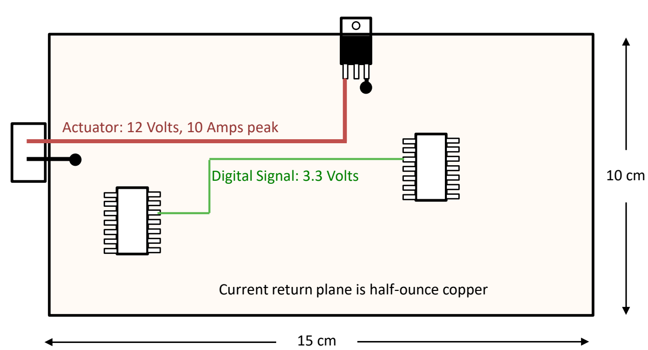
Basic Calculations

Common Impedance Coupling in on a Circuit Board

Two circuits use the same circuit board ground plane as the return path for their respective currents. One circuit drives a solenoid actuator and exhibits peak currents as high as 10 amps. The other circuit is a 3.3-V digital signal. The half-ounce copper ground plane is 10 cm x 15 cm. Calculate the maximum voltage in the digital circuit resulting from common impedance coupling from the actuator circuit.



Resistance of half-ounce copper is < 1 mΩ/square

End-to-End resistance of board: < 1.5 mΩ

Voltage induced by common-impedance coupling: < 15 mV

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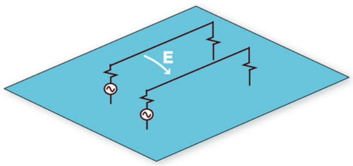
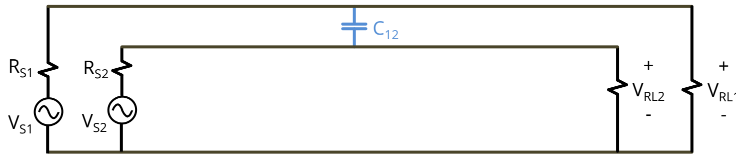
Electric Field Coupling

aka: Capacitive Coupling





- Requires 0 conductor connections between the source and victim.
- Coupling proportional to dV/dt.
- Most likely to be dominant at higher frequencies.
- Most likely to be dominant when sources are high impedance (high voltage) circuits.

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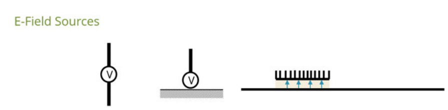
Electric Field Coupling



Examples

- Coupling from circuit board heatsinks to cables or enclosures
- AM radio interference from overhead power lines
- Automotive component noise picked up by the rod antenna in CISPR 25 “radiated” emissions tests
- Microprocessor resets due to indirect electrostatic discharges

Solutions

- Eliminate electric field coupling by reducing the voltage of the source
- Reduce the impedance of the victim circuit
- Increase the distance between source and victim
- Redirect or interrupt the field using electric field shielding
- Isolate signals in frequency by filtering
- Isolate signals in time

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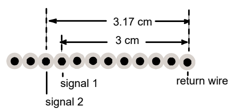
Basic Calculations

Capacitive Coupling in a Ribbon Cable

A 10-ohm function generator sends a 1-volt, 3.0-MHz sine wave to a 300-ohm load through a 0.75-meter ribbon cable. The return wire (ground) is 3.0 cm away from the signal wire in the same ribbon cable. The radius of each wire in the ribbon cable is 0.32 mm. Another wire in the same cable is located 0.17 cm away from the first signal wire. This wire is also attached to a 10-ohm source and a 300-ohm load and uses the same return (ground) wire as the first circuit. The relative permittivity of the insulation is 2.0. Calculate the coupled voltage and amount of crosstalk (in dB) due to capacitive coupling between the two circuits at 3.0 MHz.



$$C_{12} = \frac{\pi\varepsilon\ell}{\cosh^{-1}\left(\frac{d}{2a}\right)} = \frac{\pi(2.0)(8.854\times10^{-12}\ \text{F/m})(0.75\ \text{m})}{\cosh^{-1}\left(\frac{1.7\ \text{mm}}{0.64\ \text{mm}}\right)} = 25.6\ \text{pF}$$

$$|V_{RL2}| = V_{RL1}\left|\frac{R_L\,||\,R_S}{R_L\,||\,R_S + j\left(\frac{1}{\omega C_{12}}\right)}\right| = V_{RL1}\left|\frac{9.7\ \Omega}{9.7\ \Omega + j\left(\frac{1}{2\pi(3\times10^{6}\ \text{Hz})(25.6\times10^{-12}\ \text{F})}\right)}\right|$$

$$= V_{RL1}\left|\frac{9.7\ \Omega}{9.7\ \Omega + j2072}\right|$$

$$= 4.7\times10^{-3}V_{RL1} = 4.7\ \text{mV}$$

$$\text{Xtalk}_{21} = 20\log\left|\frac{V_{RL2}}{V_{RL1}}\right| = 20\log\left|4.7\times10^{-3}\right| = -47\ \text{dB}$$

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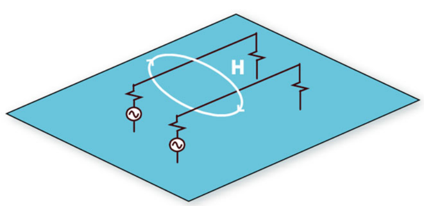
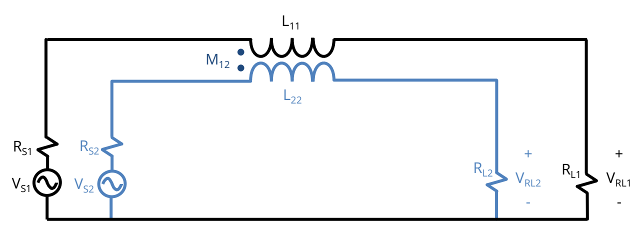
Magnetic Field Coupling

aka: Inductive Coupling





- Requires 0 conductor connections between the source and victim.
- Coupling proportional to dI/dt.
- Most likely to be dominant at higher frequencies.
- Most likely to be dominant when sources are low impedance (high current) circuits.

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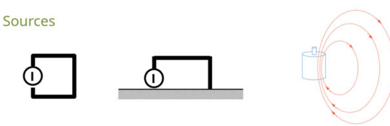
Magnetic Field Coupling

H-Field Sources



Examples

- LF coupling from power transformers or motors
- Coupling from solenoids or low-gauge wires
- LF noise in a handheld AM radio

Solutions

- Eliminate magnetic field coupling by reducing the currents in the source
- Increase the distance between source and victim
- Redirect the field using magnetic field shielding
- Isolate signals in frequency by filtering
- Isolate signals in time

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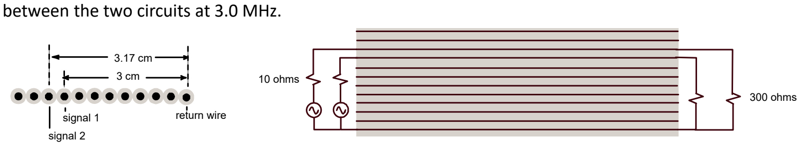
Basic Calculations

Inductive Coupling in a Ribbon Cable

A 10-ohm function generator sends a 1-volt, 3.0-MHz sine wave to a 300-ohm load through a 0.75-meter ribbon cable. The return wire (ground) is 3.0 cm away from the signal wire in the same ribbon cable. The radius of each wire in the ribbon cable is 0.32 mm. Another wire in the same cable is located 0.17 cm away from the first signal wire. This wire is also attached to a 10-ohm source and a 300-ohm load and uses the same return (ground) wire as the first circuit. The relative permittivity of the insulation is 2.0. Calculate the coupled voltage and amount of crosstalk (in dB) due to inductive coupling between the two circuits at 3.0 MHz.



$$L_{11} = \frac{\mu_0 \ell}{\pi}\cosh^{-1}\left(\frac{d}{2a}\right) = \left(4\times10^{-7}\ \text{H/m}\right)\left(0.75\ \text{m}\right)\cosh^{-1}\left(\frac{30\ \text{mm}}{0.64\ \text{mm}}\right) = 1.36\ \mu\text{H}$$

$$L_{22} = \frac{\mu_0 \ell}{\pi}\cosh^{-1}\left(\frac{d}{2a}\right) = \left(4\times10^{-7}\ \text{H/m}\right)\left(0.75\ \text{m}\right)\cosh^{-1}\left(\frac{31.7\ \text{mm}}{0.64\ \text{mm}}\right) = 1.38\ \mu\text{H}$$

$$L_{12} = kL_{22} \approx \frac{3.0}{3.17} 1.38\ \mu\text{H} = 1.3\ \mu\text{H}$$

(This is slightly high. Anywhere from 1 μH to 1.3 μH is a good estimate.)

$$\left|V_{RL2}\right| = \left|j\omega L_{12} I_1\right|\left(\frac{300}{300+10}\right) = \left|2\pi\left(3\times10^{6}\ \text{Hz}\right)\left(1.3\times10^{-6}\ \text{H}\right)\frac{V_{RL1}}{300}\right|\left(\frac{300}{300+10}\right)$$

$$= 7.9\times10^{-2}\, V_{RL1}$$

$$\text{Xtalk}_{21} = 20\log\left|\frac{V_{RL2}}{V_{RL1}}\right| = 20\log\left|7.9\times10^{-2}\right| = -22\ \text{dB}$$

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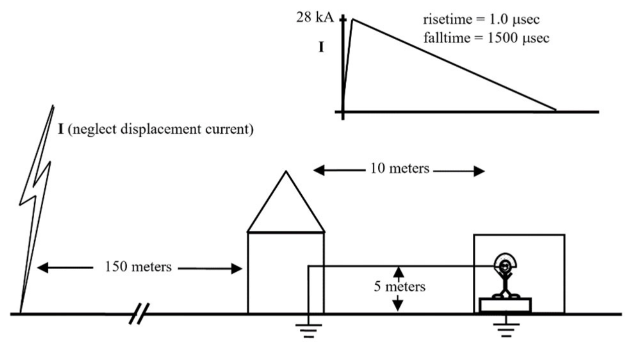
Basic Calculations

H-field Coupling from Lightning to Electrically Small Circuit

Holly Homeowner decides to put a wireless access point in her garage. She buys a bundle of the best shielded Ethernet cable she can find and strings it from the roof of her house to the roof of the garage 10 meters away. After hooking up the cable on the house side and making sure the shield of the cable is well grounded, she runs over to the garage to hook up the phone. As she holds on to the cable, there is a stroke of lightning 0.15 kilometers west of the house. Modeling the lightning stroke as an infinite current element, what is the voltage induced across Holly due to the magnetic field coupling?



$$
\begin{aligned}
V_{Holly} &= -\partial\Psi/\partial t \\
&\approx -\partial/\partial t\left[\mu_0 H(\text{Area of loop})\right] \\
&\approx -\partial/\partial t\left[\mu_0\left(\frac{I}{2\pi r}\right)(10\text{ meters}\times 5\text{ meters})\right] \\
&\approx -\partial I/\partial t\left[\left(\frac{4\pi\times10^{-7}\text{ H/m}}{2\pi\times155\text{ meters}}\right)(50\text{ m}^2)\right] \\
&\approx -\partial I/\partial t\left[6.45\times10^{-8}\text{ Henries}\right] \\
&\approx \begin{cases} -6.45\times10^{-8}\left(\dfrac{28\times10^{3}\text{ A}}{1\times10^{-6}\text{ sec}}\right) & 0<t<1\mu\text{sec} \\ -6.45\times10^{-8}\left(\dfrac{-28\times10^{3}\text{ A}}{1500\times10^{-6}\text{ sec}}\right) & 1\mu\text{sec}\le t\le 1501\mu\text{sec} \\ 0 & \text{otherwise} \end{cases} \\
&\approx \begin{cases} -1.8\times10^{3}\text{ volts} & 0<t<1\mu\text{sec} \\ 1.2\text{ volts} & 1\mu\text{sec}\le t\le 1501\mu\text{sec} \\ 0 & \text{otherwise} \end{cases}
\end{aligned}
$$

Radiation Coupling

- Requires 0 conductor connections between the source and victim.
- Source and victim MUST be far apart (e.g.; greater than a wavelength).
- Most likely to be dominant at higher frequencies.
- Requires something that behaves like an antenna on both the source and the victim.

Radiated Coupling

Examples

- Operation of ECU interferes with wireless communications
- Coupling from distant cell phone or FM radio towers
- Failure to meet FCC or CISPR 22 radiated emissions requirements above 100 MHz
- Device failures caused by a wireless cell phone or DSRC transmissions

Solutions

- Reduce efficiency of the unintentional antenna
- Reduce coupling between antenna and the source/victim
- Isolate signals in frequency by filtering
- Isolate signals in time

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Analog, Digital and Power Circuits

Analog

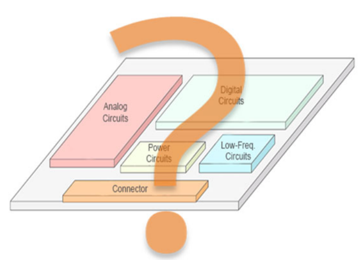
- Analog audio and video signals
- Temperature, humidity, pressure, and position sensors
- Solenoids, motors, heaters and other actuators
- Receiving antenna signals (e.g., radio receivers, GPS, WiFi)
- Transmitting antenna signals (e.g., handheld transceivers, WiFi, phones)

Digital

- ON/OFF signals (e.g., enable, reset, status)
- Low-speed communications (e.g., RS232, I2C, CAN)
- Medium-speed communications (e.g., USB, HDMI, CAN FD, A2B)
- High-speed communications (e.g., 10GBASE-T, GDDR6X DRAM)

Power

- Low-voltage AC or DC power distribution
- High-voltage AC or DC power distribution
- Motor drivers
- Solenoid drivers
- Heating or cooling circuits



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EMC Design Guidelines

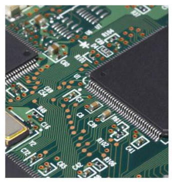
EMC Design Guideline Collection

Over the past 25 years, we've had opportunities to work with a wide variety of companies to solve circuit-board or system-level EMC problems. During this time, we've encountered all kinds of EMC design rules. Some of them are helpful, some not-so-helpful, and some practically guarantee that your product will have EMC problems.

Some people collect coins or stamps. We like to collect EMC design guidelines.

We've published our favorite EMC design rules (the good, the bad and the ugly) on this web site. Rules on this site were collected primarily from lists maintained by companies for internal use. Additional rules were gleaned from published books, technical papers and application notes. Please note that LearnEMC does not endorse any of the EMC design rules (we prefer to call them "guidelines") on this site. Like stamps or coins, our collection is being put on display for your information and entertainment. We hope you enjoy it!

- Why You Should Be Cautious About Using EMC Design Guidelines
- The Most Important EMC Design Guidelines
- Other Good EMC Design Guidelines
- Not-So-Good EMC Design Guidelines
- Some of the Worst EMC Design Guidelines
- Effective Application of EMC Design Guidelines
- Commercial EMC Rule Checkers



If you have a guideline that you'd be willing to share, please email it to info@LearnEMC.com. Be sure to indicate the source. We'd like to hear from you.

Updates or corrections to this web page should be emailed to webmaster@LearnEMC.com.
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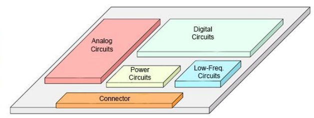
Some of the Worst EMC Design Guidelines

These guidelines tend to cause more EMC problems than they prevent.

Circuit Board Layout

Circuits on a printed circuit board should be grouped by type with power circuits closest to the connector and high-speed digital circuit furthest from the connector.

This design guideline (or variants that indicate other groupings) is probably responsible for more crazy board layouts than any other individual EMC design guideline. It ignores the fundamental idea that different boards have different functions. We have seen boards with very high speed digital signals routed all the way across the board in an attempt to keep the digital components away from the connector.



It is certainly important to consider the function and speed of components when deciding where to place them. However, any general statements about placement relative to the connector are more likely to produce a bad design than a good one. Usually, but not always, it's a good idea to put the components that send or receive signals through the connector nearest the connector. Placement is important, but design guidelines that dictate placement without considering the function and signals associated with the circuits are very dangerous.

Solid ground planes should be gapped between analog and digital circuits.

Probably a close second in the competition for the worst EMC design guideline every conceived. There a some (very few) situations where gapping a ground plane between analog and digital circuits is a good idea. These situations are

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Key Points

- **Don't rely on EMC Design Guidelines**
- Be familiar with currents and current paths
- Learn to recognize good EMI sources
- Learn to recognize good antennas
- Be aware of fundamental EMI radiation mechanisms

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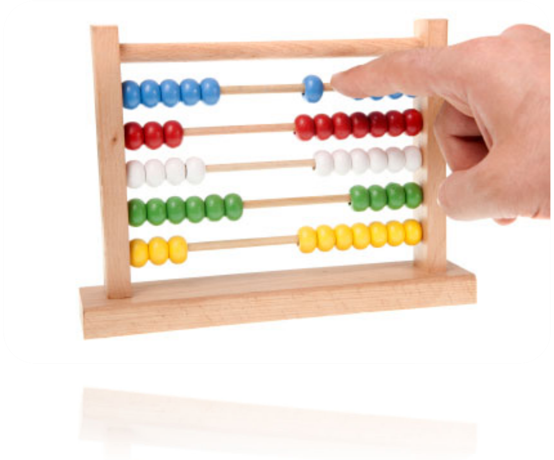
Important to Keep in Mind

"A rough estimate of the **dominant EMI problem** is more useful than a precise calculation of a **negligible problem**."

Prof. Tom Van Doren



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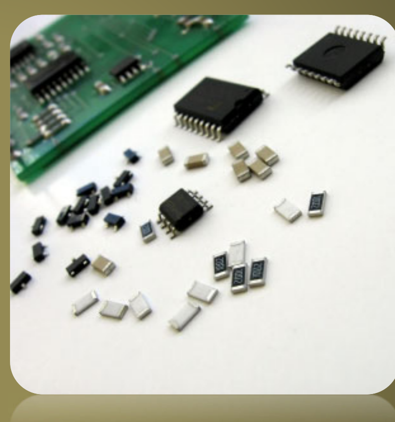
Electromagnetic Compatibility Principles and Design

Circuit Components and Parasitics



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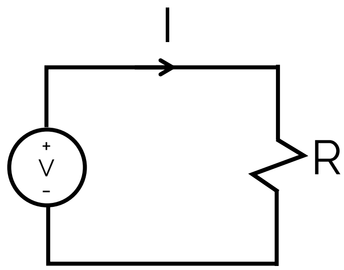
Voltage, Current and Resistance



Ohm's Law: $V = I \times R$

- Circuit designers normally neglect the resistance of the connecting wires.
- EMC and signal integrity engineers must be able to quickly assess the resistance of various conductors and determine when these resistances are negligible and when they are critically important.

Resistance

For a conductor with a uniform current distribution:

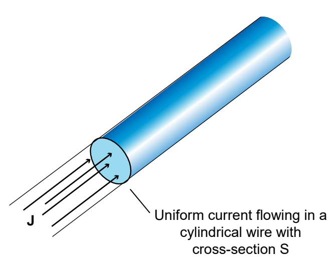
$$\vec{J} = \sigma \vec{E}$$

$$\int_S \left|\vec{J} \times \overrightarrow{ds}\right| = \int_S \sigma \left|\vec{E} \times \overrightarrow{ds}\right|$$

$$I = \sigma \left|E\right| A$$

$$I = \sigma A \frac{V}{\ell}$$

$$\frac{V}{I} = \frac{\ell}{\sigma A}$$



$$R = \frac{\ell}{\sigma A} \quad \text{ohms}$$

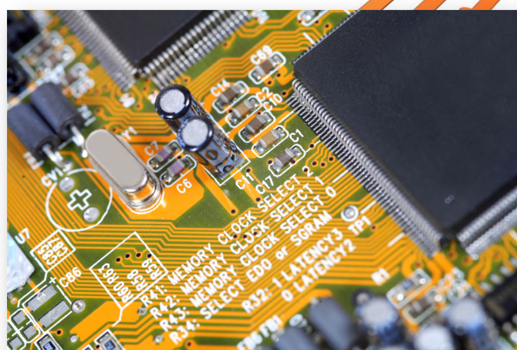
Quiz Question

The D.C. resistance of a 5-cm trace on a printed circuit board is,

a. more than an ohm

b. less than an ohm

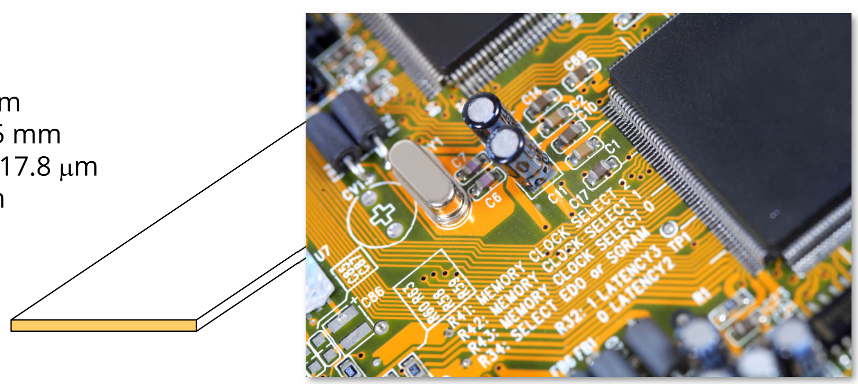
c. about 1 ohm



DC Resistance of a Printed Circuit Board Trace

$R = \frac{\ell}{\sigma A}$ ohms

Trace length = 5 cm
Trace width = 0.25 mm
Trace thickness = 17.8 μm
σ_{cu} = 5.8 x 10^7 S/m



$$R = \frac{0.05\ \text{m}}{(5.8 \times 10^{7}\ \text{S/m})(0.25\text{x}10^{-3}\ \text{m})(17.8\text{x}10^{-6}\ \text{m})} = 0.19\ \text{ohms}$$

Resistance per meter of #24 Telephone Wire

At low frequencies:

$$R = \frac{\ell}{\sigma A} = \frac{\ell}{\sigma_{Cu}\pi a^2} = \frac{1\,\text{m}}{\left(5.8\text{x}10^7\,\text{S/m}\right)\left[\pi\left(0.000256\,\text{m}\right)^2\right]} = 84\,\text{m}\Omega/\text{m}$$

Radius of #24 round wire

Conductivity of copper (and approximate conductivity of most excellent conductors)

Metal	Conductivity (σ) in siemens/m
Copper	5.8 x 10^7
Silver	6.3 x 10^7
Gold	4.1 x 10^7
Aluminum	3.5 x 10^7
Steel	~2 x 10^6
Sea Water	4.8

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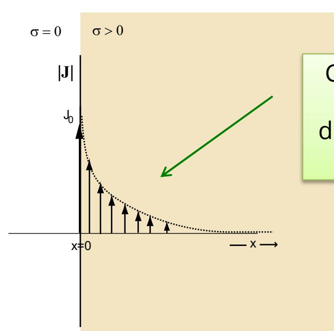
Skin Depth

At high frequencies, electric fields can't penetrate good conductors very well.

$$\vec{J} = \sigma\vec{E} \quad \text{amps/m}^2$$

Relationship between conduction current density and electric field



Current density falls off exponentially with distance from conductor surface.

$$\left|\vec{J}_s\right| = J_0 e^{-\left(\sqrt{\pi f\mu\sigma}\right)x} = J_0 e^{-x/\delta} \quad \text{amps/m}$$

where skin depth is defined as: $\delta = \frac{1}{\sqrt{\pi f\mu\sigma}}$ meters

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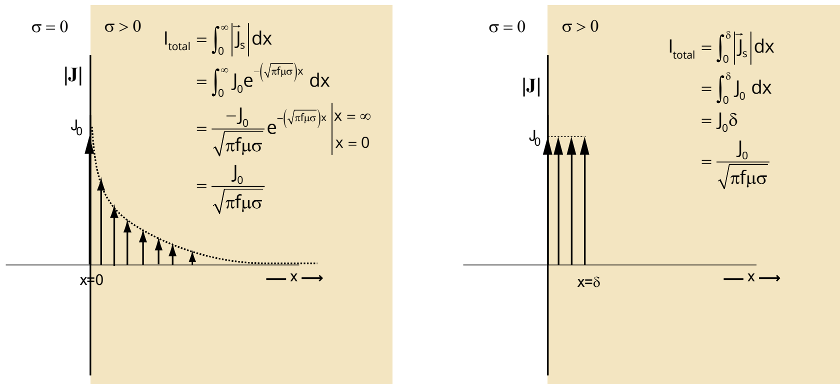
Skin Depth

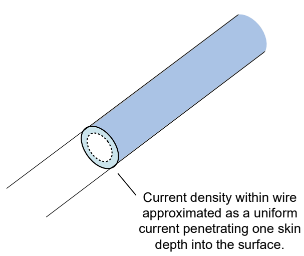
The total current in the conductor can be determined by integrating the current density from the surface to planes deep within the conductor.



The total current is equal to the current that would flow if the current density on the surface remained constant for one skin depth, then suddenly dropped to zero.

Skin Depth

For the purposes of calculating resistance, conductors that are several skin depths thick can be modeled as though they carry a uniform current that penetrates one skin depth in from the conductor surface.



Actual cross-sectional area:

$$A = \pi a^2$$

Effective cross-sectional area:

$$A = \left[\pi a^2\right] - \left[\pi(a-\delta)^2\right]$$
$$\approx 2\pi a \delta \quad \text{for } \delta \ll a$$

At high frequencies, where current carrying conductors are several skin depths thick, the effective cross-sectional area is less than the actual cross-sectional area of the conductor. This increases the resistance of the conductor.

Skin Depth in Copper

Frequency	Skin Depth
DC	∞
60 Hz	8.6 mm
100 Hz	6.7 mm
1 kHz	2.1 mm
10 kHz	670 μm
100 kHz	210 μm
1 MHz	67 μm
10 MHz	21 μm
100 MHz	6.7 μm
1 GHz	2.1 μm

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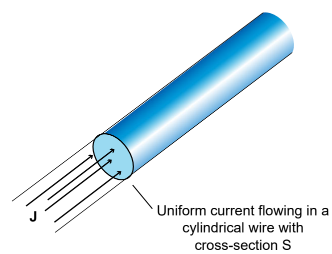
Resistance

At low frequencies:

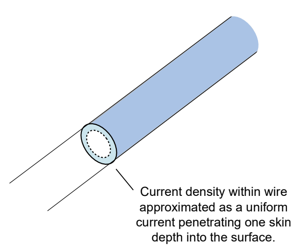
$$R = \frac{\ell}{\sigma A} \quad \text{ohms}$$



At high frequencies:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \quad \text{meters}$$

$$R \approx \frac{\ell}{\sigma 2 \pi a \delta} \quad \text{ohms}$$



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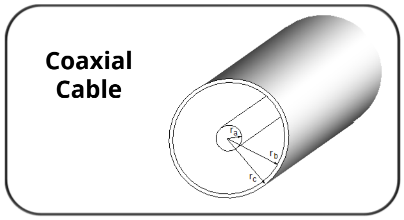
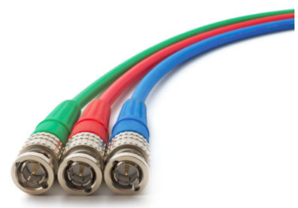
Examples

RG58 Coaxial Cable



Outer conductor diameter:	4.2 mm
Inner conductor diameter:	1.2 mm
Dielectric permittivity:	2.3

Propagation Delay:	5.0 nsec/m
Characteristic Impedance:	50 Ω
Capacitance per unit length:	100 pF/m
Inductance per unit length:	250 nH/m
Resistance per unit length:	90 mΩ/m @1 MHz
Cable Attenuation at 1 MHz:	7.8 dB/km @1 MHz



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Resistance per meter of RG58 Coaxial Cable

At low frequencies:

$$R_{inner} = \frac{\ell}{\sigma_{Cu}\pi a^2} = \frac{1\,\text{m}}{\left(5.7\text{x}10^7\ \text{S/m}\right)\left[\pi\left(0.00061\text{m}\right)^2\right]} = 15\ \text{m}\Omega/\text{m}$$

$$R_{outer} \approx \frac{\ell}{\sigma_{Cu}\left(2\pi a\right)\text{shieldthickness}} = \frac{1\,\text{m}}{\left(5.7\text{x}10^7\ \text{S/m}\right)2\pi\left(0.0021\text{m}\right)\left(0.74\text{x}10^{-3}\ \text{m}\right)} = 18\text{m}\Omega/\text{m}$$

$$R_{total} = R_{inner} + R_{outer} = 33\text{m}\Omega/\text{m}$$

At 1 MHz: $\delta = 66\text{x}10^{-6}$ meters

$$R_{inner} \approx \frac{\ell}{\sigma_{cu}2\pi a\delta} = \frac{1\,\text{m}}{\left(5.8\text{x}10^7\ \text{S/m}\right)2\pi\left(0.0006\text{m}\right)\left(66\text{x}10^{-6}\,\text{m}\right)} = 69\ \text{m}\Omega/\text{m}$$

$$R_{outer} \approx \frac{\ell}{\sigma_{cu}2\pi a\delta} = \frac{1\,\text{m}}{\left(5.8\text{x}10^7\ \text{S/m}\right)2\pi\left(0.0021\text{m}\right)\left(66\text{x}10^{-6}\,\text{m}\right)} = 20\ \text{m}\Omega/\text{m}$$

$$R_{total} = R_{inner} + R_{outer} = 89\text{m}\Omega/\text{m}$$

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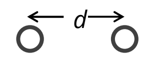
Examples

CAT5e TWP

Parallel Wires



wire radius: *a*

Conductor diameter:	0.511 mm
Conductor separation:	1.0 mm
Dielectric permittivity:	2.4

Propagation Delay:	5.2 nsec/m
Characteristic Impedance:	100 Ω
Capacitance per unit length:	52 pF/m
Inductance per unit length:	520 nH/m
Resistance at 1 MHz:	329 mΩ/m
Cable Attenuation at 1 MHz:	14 dB/km

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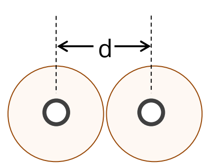
Resistance per meter of #24 Twisted Wire Pair



wire radius: a

$d = 1.0\,\text{mm}$

$a = 0.256\,\text{mm}$

Resistance of one wire at 1 MHz:

$$R \approx \frac{\ell}{\sigma 2\pi a \delta} = \frac{1\,\text{m}}{\left(5.8\text{x}10^{7}\,\text{S/m}\right)2\pi\left(0.000256\,\text{m}\right)\left(66\text{x}10^{-6}\,\text{m}\right)} = 162\,\text{m}\Omega/\text{m}$$

Resistance of two wires at 1 MHz:

$$R = 2 \times 162\ \text{m}\Omega/\text{m} = 324\,\text{m}\Omega/\text{m}$$

Wire Pair Resistance

Twisted Wire Pair Resistance

$$\begin{aligned} R &= R_{\text{wire pair}} \times \text{Twist Factor} \\ &= 324\,\text{m}\Omega/\text{m} \times 1.017 \\ &= 330\,\text{m}\Omega/\text{m} \end{aligned}$$

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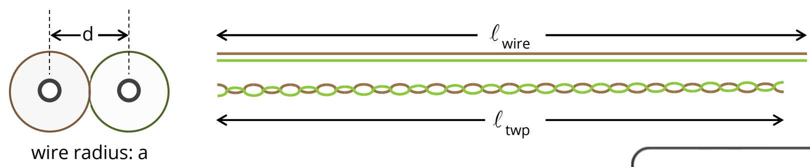
Twist Factor

If you take two parallel wires and twist them together, the length of the twisted wire pair will be shorter than the lengths of the untwisted wire.



$$\text{Twist Factor} = \frac{\ell_{wire}}{\ell_{twp}}$$

The twist factor is generally less than a few percent and is often neglected, but to get a high degree of accuracy, per-unit-length parameters calculated for parallel wires should be multiplied by the twist factor to get the per-unit-length parameters for a twisted wire pair.

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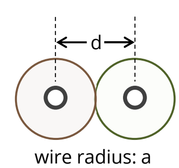
CAT 5e Twist Factor Calculation

TWP Color	Turns/meter	Twist Factor
Green	65.2	1.018
Blue	64.8	1.018
Orange	56.2	1.016
Brown	51.7	1.016

$$\text{Twist Factor} = \frac{\ell_{wire}}{\ell_{twp}} = (\text{turns per meter})\sqrt{(\pi d)^2 + \left(\frac{1}{\text{turns per meter}}\right)^2}$$



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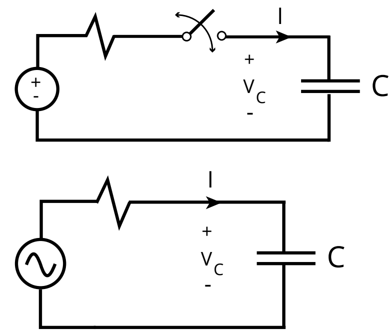
Circuit Representation of Capacitance



$$I = C\frac{dV}{dt} \quad \text{amperes}$$

$$I = j\omega C\,V \quad \text{amperes}$$

Power Dissipated in Capacitor: 0 watts
Energy Stored in Capacitor: ½ CV^2 joules (watt-sec)

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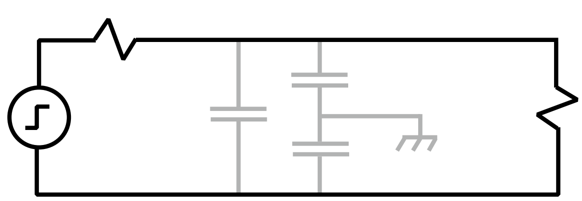
Parasitic Capacitance



- Circuit designers normally neglect the self and mutual capacitances of the connecting wires.
- EMC and signal integrity engineers must be able to quickly assess the capacitance of various conductors and determine when these capacitances are negligible and when they are critically important.

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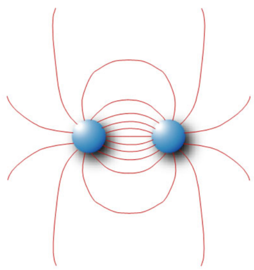
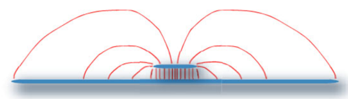
Voltage, Capacitance and Electric Fields

Any two conductors at different voltages have an electric field between them!





$$V_{ab} = \int_a^b \vec{E} \cdot \overrightarrow{d\ell}$$

When does this apply? **ALWAYS!**

Why is this important?

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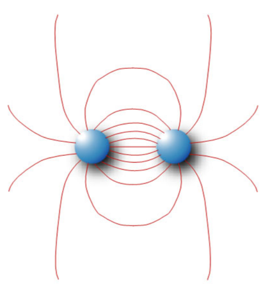
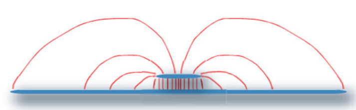
Capacitance / Electric Fields

Changing the voltage means changing the energy stored in the electric field.





$$W_E = \iiint_v \frac{1}{2} \varepsilon |E|^2 \, dv$$

Therefore, we cannot change the voltage between two conductors without adding or subtracting energy from the system.

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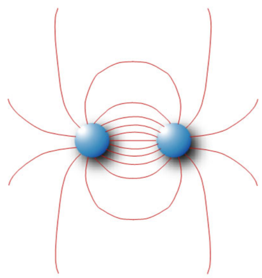
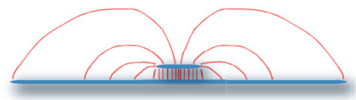
Capacitance / Electric Fields

Capacitance is the ratio of the charge on the conductors to the voltage between them.





$$C = Q/V$$

1 coulomb per volt is 1 farad

$$W_E = \frac{1}{2}CV^2$$

Therefore, capacitance is effectively a measure of how difficult it is to change the voltage between two conductors.

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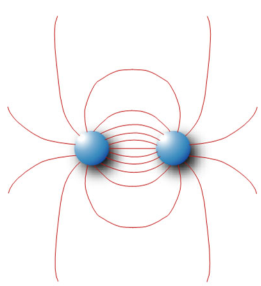
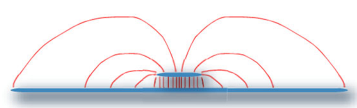
Voltage, Capacitance and Electric Fields

Capacitance is the ratio of the charge on the conductors to the voltage between them.





$$C = Q/V$$

1 coulomb per volt is 1 farad

$$W_E = \frac{1}{2}CV^2$$

Therefore, capacitance is effectively a measure of how difficult it is to change the voltage between two conductors.

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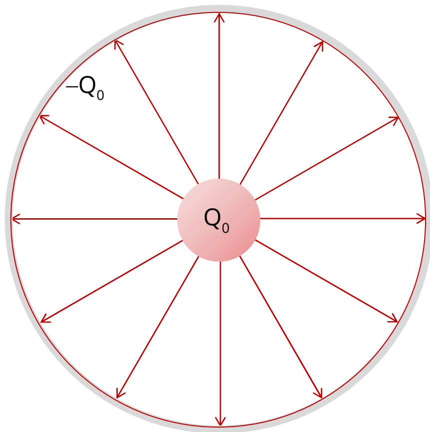
Capacitance of Concentric Spheres



$$\vec{E} = \frac{Q_0}{4\pi\varepsilon_0 r^2}\hat{r}, \quad r_a < r < r_b \quad \text{volts/m}$$

$$V_{ab} = \int_{r_a}^{r_b} \frac{Q_0}{4\pi\varepsilon_0 r^2}\,dr$$
$$= \frac{Q_0}{4\pi\varepsilon_0}\left[\frac{1}{r_a} - \frac{1}{r_b}\right] \quad \text{volts}$$

$$C_{ab} = \frac{Q_0}{V_{ab}} = \frac{4\pi\varepsilon_0}{\left[\frac{1}{r_a} - \frac{1}{r_b}\right]} \quad \text{farads}$$

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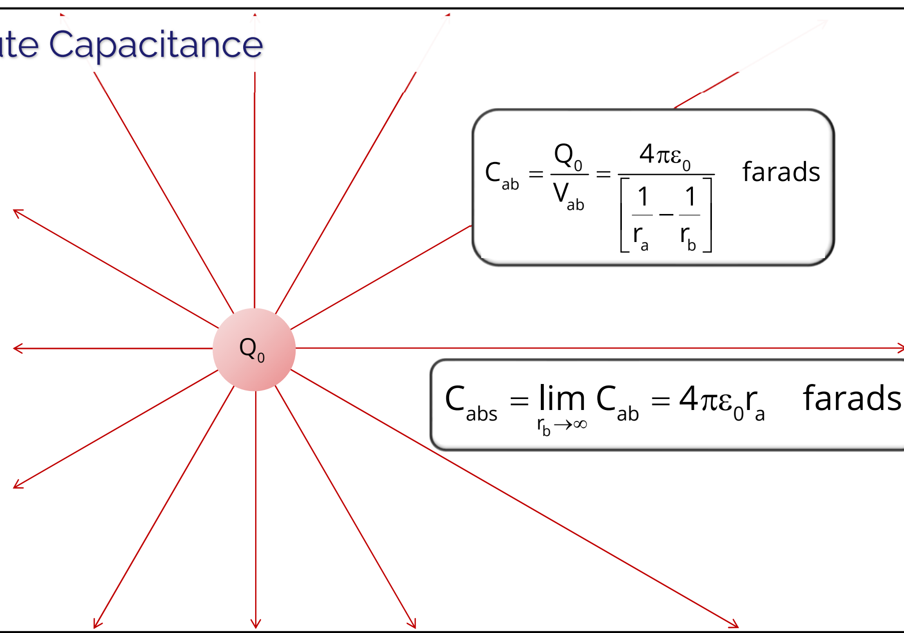
Absolute Capacitance



$$C_{ab} = \frac{Q_0}{V_{ab}} = \frac{4\pi\varepsilon_0}{\left[\frac{1}{r_a} - \frac{1}{r_b}\right]} \quad \text{farads}$$

$$C_{abs} = \lim_{r_b \to \infty} C_{ab} = 4\pi\varepsilon_0 r_a \quad \text{farads}$$

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Absolute Capacitance Calculations

Permittivity of free space: $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m

Marble: r_a = 1 cm

$$C_{abs} = 4\pi\varepsilon_0 r_a = 1.1\,\text{pF}$$

Extruded Marble

$$C_{abs} > 1.1\,\text{pF}$$

Flat Disk: r_a = 1 cm

$$C_{abs} < 1.1\,\text{pF}$$

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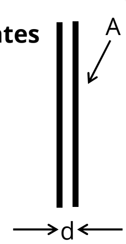
Capacitance / Electric Fields

Capacitance of Common Geometries

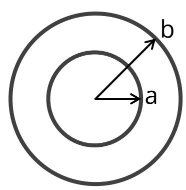
Parallel Plates

$$C = \frac{\varepsilon A}{d}$$



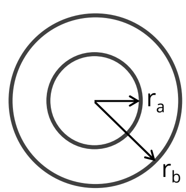
Concentric Cylinders

$$C = \frac{2\pi\varepsilon L}{\ln\left(b/a\right)}$$



Concentric Spheres

$$C = 4\pi\varepsilon\left[\frac{1}{r_a} - \frac{1}{r_b}\right]^{-1}$$



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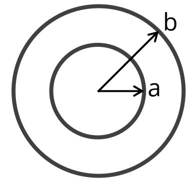
Capacitance / Electric Fields

Capacitance per Unit Length of Common Geometries

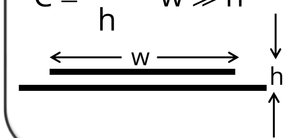
Coaxial Cable

$$C = \frac{2\pi\varepsilon}{\ln\left(b/a\right)}$$



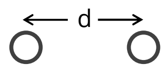
Wide Trace Over Plane

$$C = \frac{\varepsilon w}{h} \qquad w \gg h$$



Parallel Wires

$$C = \frac{\pi\varepsilon}{\cosh^{-1}\left(d/2a\right)}$$



wire radius: a

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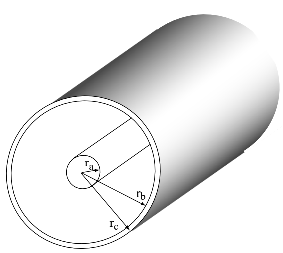
Capacitance per meter of RG58 Coaxial Cable



$r_a = 0.6\,\text{mm}$
$r_b = 2.1\,\text{mm}$

$$C = \frac{2\pi\varepsilon}{\ln\left(r_b/r_a\right)} = \frac{2\pi(2.3)\left(8.854\times10^{-12}\ \text{F/m}\right)}{\ln\left(2.1/0.6\right)} = 102\ \text{pF/m}$$

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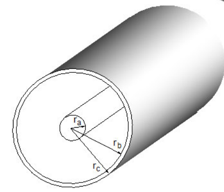
Examples

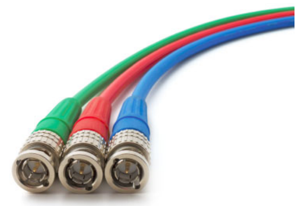
RG58 Coaxial Cable

Outer conductor diameter:	4.2 mm
Inner conductor diameter:	1.2 mm
Dielectric permittivity:	2.3

Coaxial Cable



Propagation Delay:	5.0 nsec/m
Characteristic Impedance:	50 Ω
Capacitance per unit length:	100 pF/m
Inductance per unit length:	250 nH/m
Resistance per unit length:	90 mΩ/m @1 MHz
Cable Attenuation at 1 MHz:	7.8 dB/km @1 MHz



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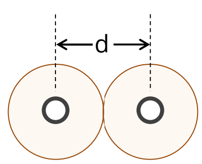
Capacitance per meter of #24 Twisted Wire Pair



wire radius: a

$d = 1.0\,\text{mm}$

$a = 0.255\,\text{mm}$

$$
\begin{aligned}
C &= \frac{\pi\varepsilon}{\cosh^{-1}\left(d/2a\right)} \\
&= \frac{\pi\left(\varepsilon_{r-\text{effective}} = 2.36\right)8.854\times10^{-12}\ \text{F/m}}{\cosh^{-1}\left(1.0/(2\times0.255)\right)} \\
&= 51\,\text{pF/m}
\end{aligned}
$$

Wire Pair Capacitance

Twisted Wire Pair Capacitance

$$
\begin{aligned}
C &= C_{\text{wire pair}} \times \text{Twist Factor} \\
&= 51\,\text{pF/m} \times 1.017 \\
&= 52\ \text{pF/m}
\end{aligned}
$$

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Examples

CAT5e TWP

Conductor diameter:	0.511 mm
Conductor separation:	1.0 mm
Dielectric permittivity:	2.36

Parallel Wires

$$C = \frac{\pi\varepsilon}{\cosh^{-1}\left(d/2a\right)}$$

d

wire radius: a

Propagation Delay:	5.2 nsec/m
Characteristic Impedance:	100 Ω
Capacitance per unit length:	52 pF/m
Inductance per unit length:	520 nH/m
Resistance at 1 MHz:	329 mΩ/m
Cable Attenuation at 1 MHz:	14 dB/km

Self and Mutual Capacitances

To calculate these self and mutual capacitances, the principle of superposition is applied. The absolute potential of each conductor can be expressed as the sum of the potentials due to charge on each of the other conductors and its own charge.

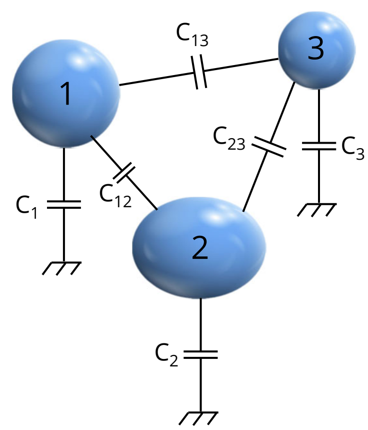
$$V_i = \sum_{j=1}^{n} p_{ij} Q_j \quad (i = 1,2,\ldots,n) \quad \text{volts,}$$

where the coefficients of potential, p_{ij}, are functions of the geometry. This equation can be written in matrix form as,

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix} = \begin{bmatrix} p_{11} & p_{12} & \cdots & p_{1n} \\ p_{21} & p_{22} & \cdots & p_{2n} \\ \vdots & \vdots & & \vdots \\ p_{n1} & p_{n2} & \cdots & p_{nn} \end{bmatrix} \begin{bmatrix} Q_1 \\ Q_2 \\ \vdots \\ Q_n \end{bmatrix}.$$

Solving this system of equations for Q results in,

$$\begin{bmatrix} Q_1 \\ Q_2 \\ \vdots \\ Q_n \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} & \cdots & c_{1n} \\ c_{21} & c_{22} & \cdots & c_{2n} \\ \vdots & \vdots & & \vdots \\ c_{n1} & c_{n2} & \cdots & c_{nn} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix}.$$



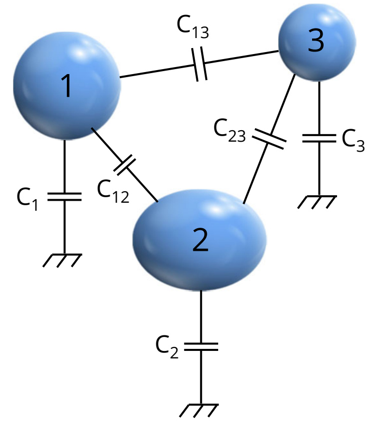
where $[c] = [p]^{-1}$ is referred to as the ***generalized capacitance matrix***.

Self and Mutual Capacitances

Self and mutual capacitance values, which are always non-negative, can be calculated from the elements of the *generalized capacitance matrix* using the relations,

$$C_i = c_{i1} + c_{i2} + \cdots + c_{in}$$
$$C_{ij} = -c_{ij}$$

Once these values have been calculated for a system of conductors, the behavior of the system can be analyzed using simple circuit modeling techniques.



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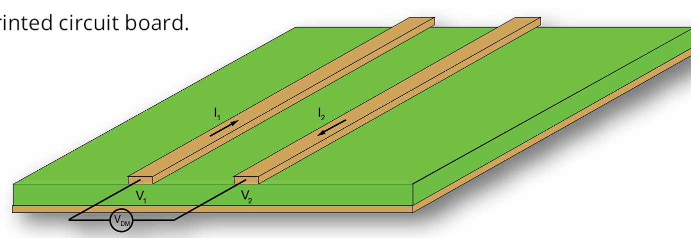
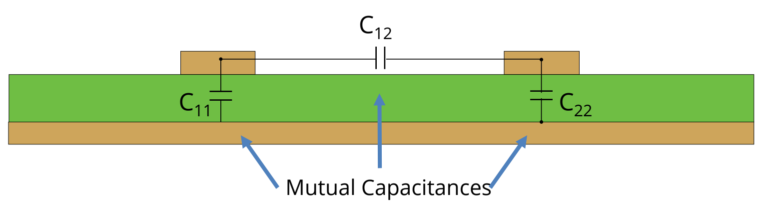
Mutual vs. Effective Capacitance

Two traces carrying a differential signal on a printed circuit board.



Effective Capacitance (or the transmission line capacitance)

$$C_{eff} = C_{12} + \frac{C_{11} + C_{22}}{C_{11}C_{22}}$$



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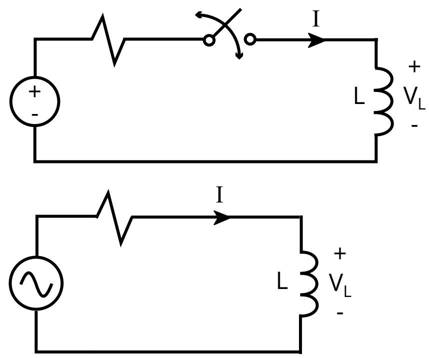
Circuit Representation of Inductance



$V_L = L\frac{dI}{dt}$ amperes

$V_L = j\omega LI$ amperes

Power Dissipated in Inductor: 0 watts
Energy Stored in Inductor: ½ LI^2 joules (watt-sec)

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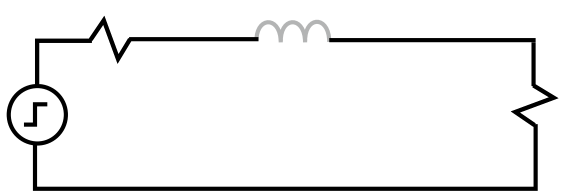
Parasitic Inductance



- Circuit designers normally neglect the self and mutual Inductances of the connecting wires.
- EMC and signal integrity engineers must be able to quickly assess the inductance of various circuits and determine when these inductances are negligible and when they are critically important.

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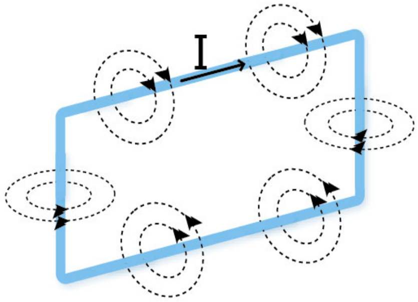
Current and Magnetic Fields



- Magnetic field lines circulate around flowing electric charge (current).
- Lines of magnetic field do not start or stop. They always close on themselves.

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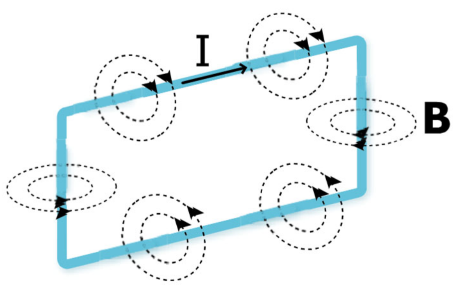
Inductance / Magnetic Fields

Every current is surrounded by a magnetic field!



$$\vec{B} = \mu \vec{H}$$

$$I_{enc} = \oint \vec{H} \cdot \vec{d\ell}$$

When does this apply? **ALWAYS!**

Why is this important?

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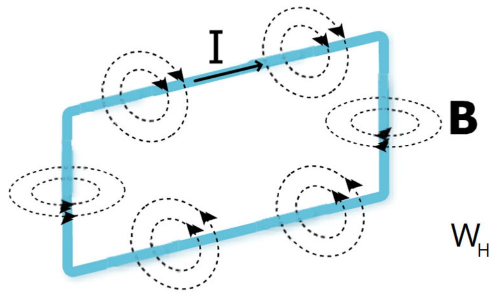
Inductance / Magnetic Fields

Changing the current means changing the energy stored in the magnetic field.

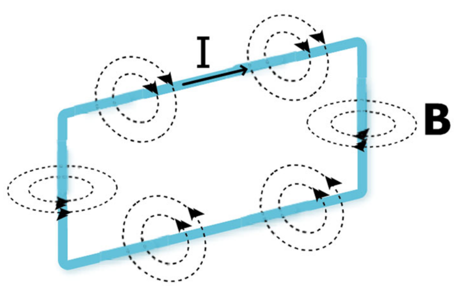


$$W_H = \iiint_v \frac{1}{2}\mu|H|^2 dv$$

Therefore, we cannot change the current flowing in a conductor without adding or subtracting energy from the system.

Inductance / Magnetic Fields

Inductance is the ratio of the total magnetic flux to the current that produced it.



$$\Psi = \int_S \vec{B} \cdot \overrightarrow{ds} \quad \text{webers}$$

$$L = \frac{\Psi}{I} \quad \text{henries}$$

$$W_H = \frac{1}{2}LI^2$$

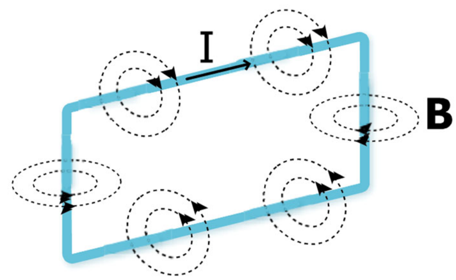
Therefore, inductance is effectively a measure of how difficult it is to change the current flowing in a circuit.

Inductance

Inductance is a property of current loops!

$$\Psi = \int_S \vec{B} \cdot \overrightarrow{ds} \quad \text{webers}$$

$$L = \frac{\Psi}{I} \quad \text{henries}$$



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Inductance / Magnetic Fields

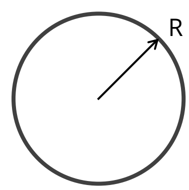
Inductance of Common Geometries

Note: These formulas assume that the loop is made of wire with a circular cross-section (with wire radius, a).

If the wire is flat with width, *w*, these equations can still be used with an effective wire radius: $a_e = 0.25w$

Circular Loop

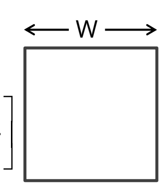
$$L \approx R\mu \left[\ln\left(\frac{8R}{a}\right) - 2.0 \right]$$



wire radius: a

Square Loop

$$L \approx \frac{2\mu W}{\pi} \left[\ln\left(\frac{W}{a}\right) - 0.774 \right]$$



wire radius: a

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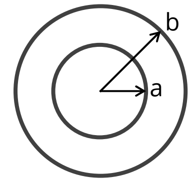
Inductance / Magnetic Fields

Inductance per Unit Length of Common Geometries

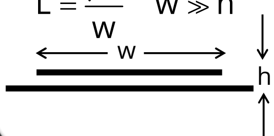
Coaxial Cable

$$L = \frac{\mu}{2\pi}\ln\left(b/a\right)$$



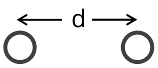
Wide Trace Over Plane

$$L = \frac{\mu h}{w} \qquad w \gg h$$



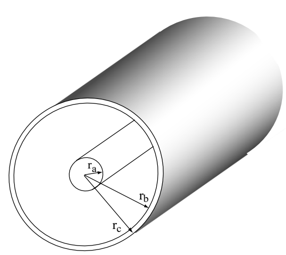
Parallel Wires

$$L = \frac{\mu}{\pi}\cosh^{-1}\left(d/2a\right)$$



wire radius: a

Inductance per meter of RG58 Coaxial Cable



$r_a = 0.6\,\text{mm}$

$r_b = 2.1\,\text{mm}$

$$\begin{aligned} L &= \frac{\mu}{2\pi}\ln\left(r_b/r_a\right) \\ &= \frac{\left(4\pi\times10^{-7}\ \text{H/m}\right)}{2\pi}\ln\left(2.1/0.6\right) \\ &= 251\,\text{nH/m} \end{aligned}$$

Examples

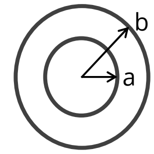
RG58 Coaxial Cable

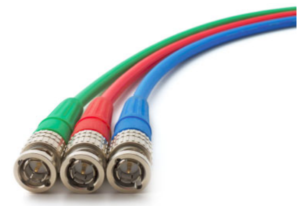
Outer conductor diameter:	4.2 mm
Inner conductor diameter:	1.2 mm
Dielectric permittivity:	2.3

Propagation Delay:	5.0 nsec/m
Characteristic Impedance:	50 Ω
Capacitance per unit length:	100 pF/m
Inductance per unit length:	250 nH/m
Resistance per unit length:	90 mΩ/m
Cable Attenuation at 1 MHz:	7.8 dB/km

Coaxial Cable

$$L = \frac{\mu}{2\pi} \ln\left(b/a \right)$$





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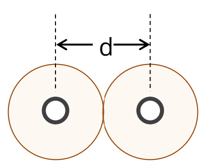
Inductance per meter of #24 Twisted Wire Pair



wire radius: a

$$d = 1.0\,\text{mm}$$
$$a = 0.255\,\text{mm}$$

$$L = \frac{\mu}{\pi} \cosh^{-1}\left(d/2a \right) s$$
$$= \frac{\left(4\pi \times 10^{-7}\ \text{H/m}\right)}{\pi} \cosh^{-1}\left(1.0 / \left(2 \times 0.255\right) \right)$$
$$= 518\ \text{nH/m}$$

Wire Pair Inductance

Twisted Wire Pair Inductance

$$L = L_{\text{wire pair}} \times \text{Twist Factor}$$
$$= 517.6\ \text{nH/m} \times 1.017$$
$$= 526\ \text{nH/m}$$

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Examples

CAT5e TWP

Parallel Wires

$L = \frac{\mu}{\pi} \cosh^{-1}\left(d / 2a \right)$

← d →

wire radius: a

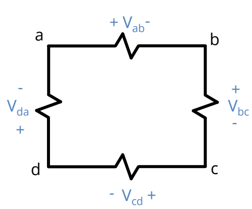
Conductor diameter:	0.511 mm
Conductor separation:	1.0 mm
Dielectric permittivity:	2.4

Propagation Delay:	5.2 nsec/m
Characteristic Impedance:	100 Ω
Capacitance per unit length:	52 pF/m
Inductance per unit length:	525 nH/m
Resistance at 1 MHz:	329 mΩ/m
Cable Attenuation at 1 MHz:	14 dB/km

Faraday's Law

A time-varying magnetic flux passing through a circuit induces a voltage in that circuit.

$$\oint \vec{E} \cdot \overrightarrow{d\ell} = -\frac{\partial}{\partial t} \int_S \vec{B} \cdot \overrightarrow{ds}$$

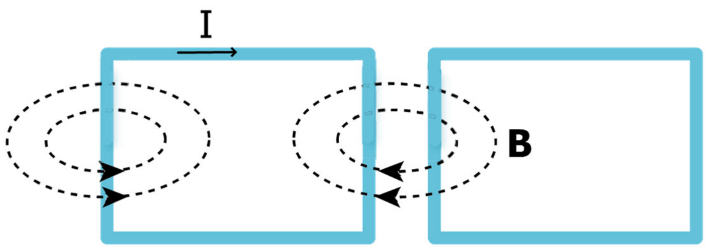


$$\int_a^b \vec{E} \cdot \overrightarrow{d\ell} + \int_b^c \vec{E} \cdot \overrightarrow{d\ell} + \int_c^d \vec{E} \cdot \overrightarrow{d\ell} + \int_d^a \vec{E} \cdot \overrightarrow{d\ell} = -\frac{\partial}{\partial t} \oint_S \vec{B} \cdot \overrightarrow{ds}$$

$$V_{ab} + V_{bc} + V_{cd} + V_{da} = -\frac{\partial}{\partial t} \oint_S \vec{B} \cdot \overrightarrow{ds}$$

$$\boxed{\sum \text{voltages dropped across components in the loop} = -\frac{\partial \Psi}{\partial t}}$$

Mutual Inductance



$$L_{21} = \frac{\Psi_{21}}{I_1} \quad \text{henries}$$

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Partial Inductance

$$L_{21} = \frac{\Psi_{21}}{I_1} \quad \text{henries}$$

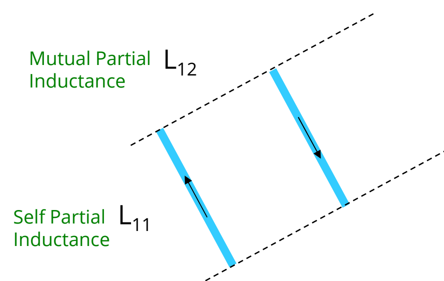
$$L_{21} = \frac{\int_{S2} \vec{B}_1 \cdot \vec{ds}}{I_1} \quad \text{henries}$$

$$L_{21} = \frac{\int_{S2} \left(\nabla \times \vec{A}_1\right) \cdot \vec{ds}}{I_1} = \frac{\oint \vec{A}_1 \cdot \vec{dl}_2}{I_1} \quad \text{henries}$$

$$L_{21} = \frac{\mu}{4\pi} \oint \oint \frac{\vec{dl}_1 \cdot \vec{dl}_2}{R} \quad \text{henries}$$

Useful for computer modeling.

Not useful for estimating inductance.



$$\vec{A}_1 = \oint \frac{\mu I_1}{4\pi R} \vec{dl} \quad \text{webers/m}$$

$$L_{ij} = \frac{\mu}{4\pi} \sum_{i=0}^{I} \sum_{i=0}^{J} I_{ij}$$

where $$I_{ij} = \int_{\text{segment } i} \int_{\text{segment } j} \frac{\vec{dl}_i \cdot \vec{dl}_j}{R_{ij}}$$

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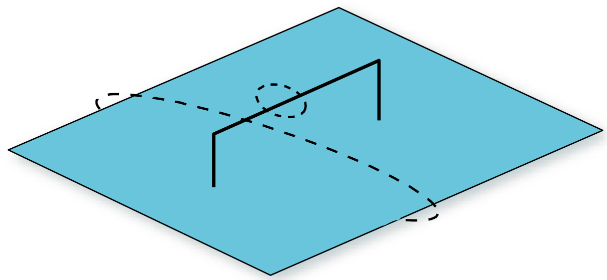
Partial Inductance (Branch Inductance)



$L_{loop} = L_{trace} + L_{via} + L_{via} + L_{plane}$

Question

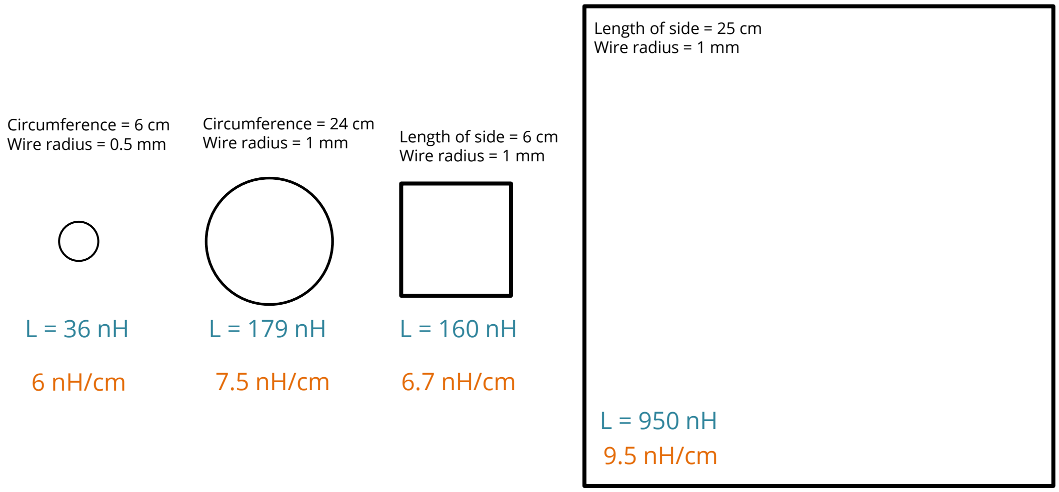
The inductance of a 2-cm wide, 10-cm long ground strap is,

a.) about 100 nanohenries

b.) 54.98 nanohenries

c.) undefined

Loop Inductances



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Inductance of a Ground Strap??

Inductance of Square Loop

$$L = \frac{2\mu_0 W}{\pi}\left[\ln\left(\frac{W}{a_e}\right) - 0.774\right] \text{ henries}$$

Inductance per unit Length of Square Loop

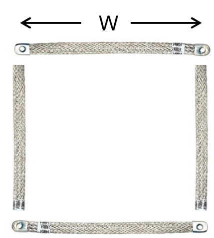
$$\frac{L}{4W} = \frac{\mu_0}{2\pi}\left[\ln\left(\frac{\text{straplength}}{0.25\times\text{strap width}}\right) - 0.774\right] \text{ henries/m}$$

$$= \frac{\mu_0}{2\pi}\left[\ln\left(4\left[\frac{\text{straplength}}{\text{strap width}}\right]\right) - 0.774\right] \text{ henries/m}$$

$$= \frac{\mu}{2\pi}\left[\ln(2) + \ln\left(\frac{2\times\text{straplength}}{\text{strap width}}\right) - 0.774\right] \text{henries/m}$$

$$\approx 2\times10^{-7}\left[\ln\left(\frac{2\times\text{straplength}}{\text{strap width}}\right)\right] \text{henries/m}$$

$$\approx 20\left[\ln\left(\frac{2\times\text{straplength}}{\text{strap width}}\right)\right] \text{nH/cm}$$



wire radius: a_e=0.25w

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Another Equation for the Inductance of a Ground Strap

What about this equation for the inductance of a ground strap?

$$L = 2\ell\left[\ln\left(\frac{2\ell}{w+t}\right) + 0.5 + 0.2235\left(\frac{w+t}{\ell}\right)\right] \text{ nH}$$

where: $\ell =$ strap length in cm.

Two things to note:

- It is based on a calculation of partial inductance. It is a relatively precise calculation of a quantity that is non-physical. (i.e., In any real application, this will not be the actual branch inductance attributable to the ground strap.)
- It yields values that are too high to be accurate in practical situations, but the same order of magnitude as results from simpler equations, such as the one on the previous slide.

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Question

The inductance of a 2-cm wide, 10-cm long ground strap that is 2 mm thick is,

a.) about 100 nH

b.) about 50 nH

c.) undefined

Branch Inductance Equation:

$$L \approx 0.20 \times \ell \times \ln\left(\frac{2\times\ell}{w}\right) \mu\text{H}$$

$$\approx 0.10 \times \left[0.20 \ln\left(\frac{0.20}{0.02}\right)\right]$$

$$\approx 46 \text{ nH}$$

Terman Equation for Self Partial Inductance:

$$L = 2\ell\left[\ln\left(\frac{2\ell}{w+t}\right) + 0.5 + 0.2235\left(\frac{w+t}{\ell}\right)\right] \text{nH}$$

$$= 20\left[\ln\left(\frac{20}{2.2}\right) + 0.5 + 0.2235\left(\frac{2.2}{10}\right)\right]$$

$$= 20\left[2.2 + 0.5 + 0.049\right]$$

$$= 55.129 \text{ nH}$$

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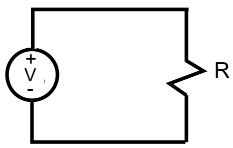
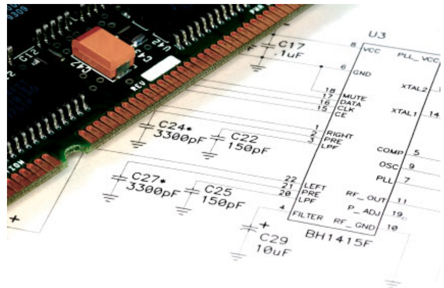
Good EMC Design is Mostly About the Things That are NOT on the Schematic



V = I x R



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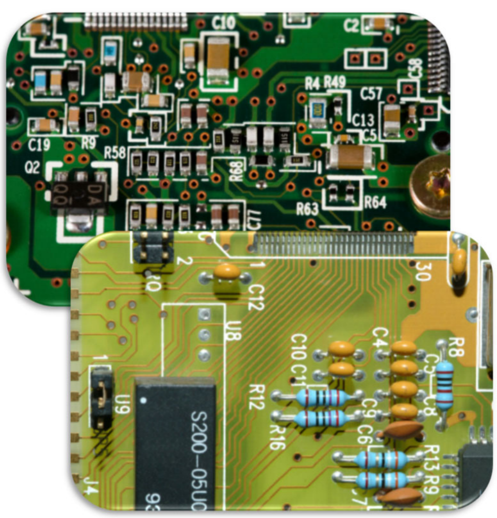
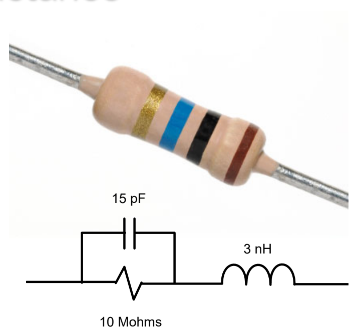
Resistors Have Capacitance and Inductance





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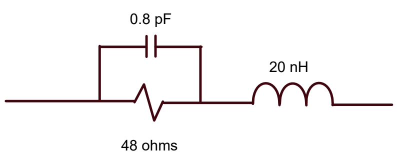
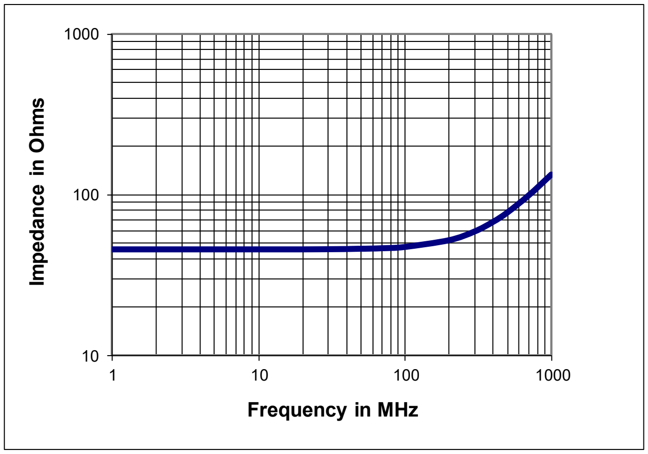
Measured Impedance of a 50-Ohm Resistor





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Types of Resistors

- Metal Film
  - High precision, low cost
- Composite
  - Medium precision, good transient immunity
- Wire Wound
  - High power, high inductance

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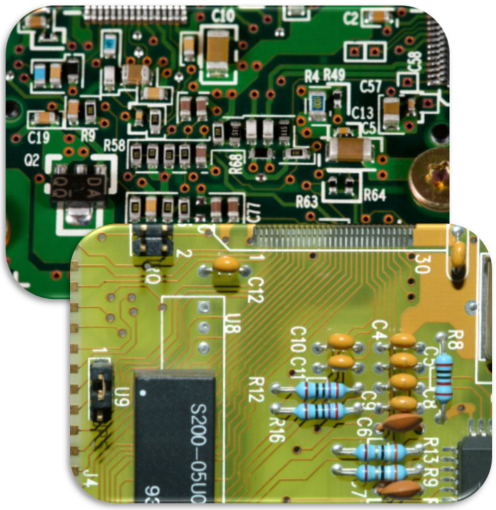
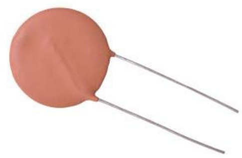
Capacitors Have Resistance and Inductance





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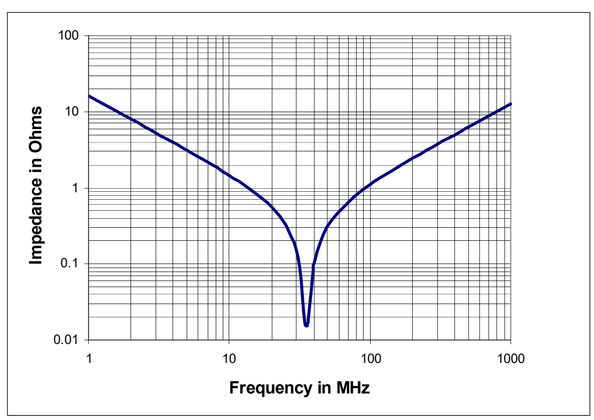
Impedance of a 0.01-µF Capacitor



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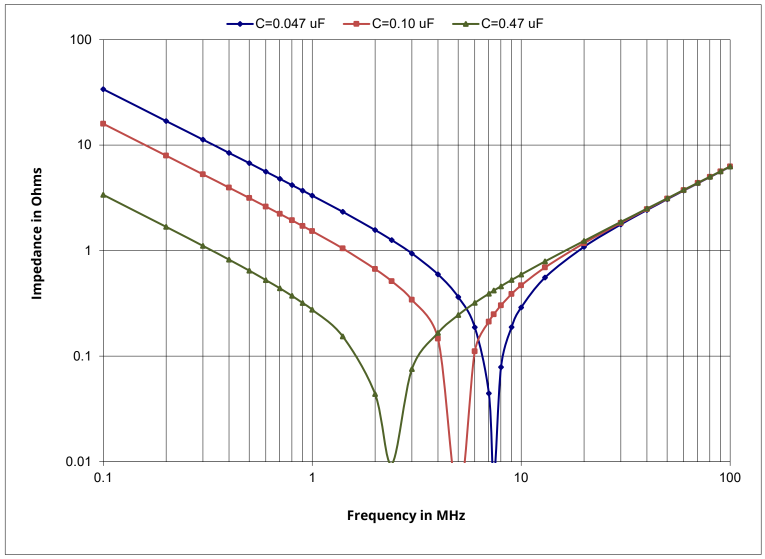
Impedance of Three Capacitors

L = 10 nH



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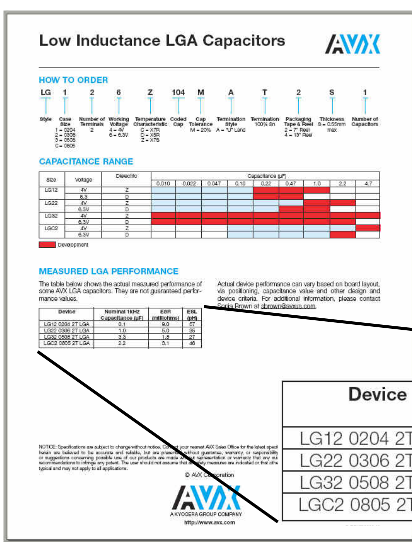
What are ESR and ESL?



Device	Nominal 1kHz Capacitance (µF)	ESR (milliohms)	ESL (pH)
LG12 0204 2T LGA	0.1	9.0	57
LG22 0306 2T LGA	1.0	5.0	35
LG32 0508 2T LGA	3.3	1.8	27
LGC2 0805 2T LGA	2.2	3.1	46

?!!

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Types of Capacitors

- Ceramic
  - Low cost, stable, good precision, low ESR
- Tantalum
  - Polarized, good energy density
- Other Electrolytic
  - Polarized, good energy density
- Film
  - Non-polarized, stable
- Mica
  - High-voltage applications

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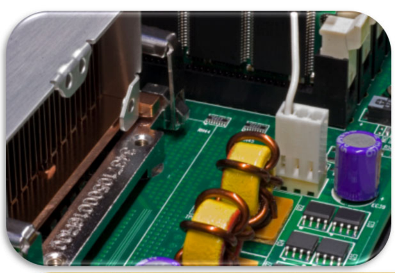
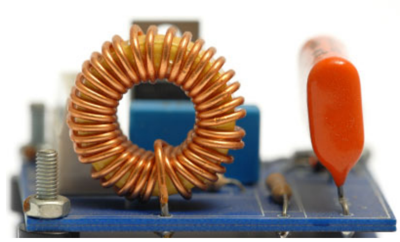
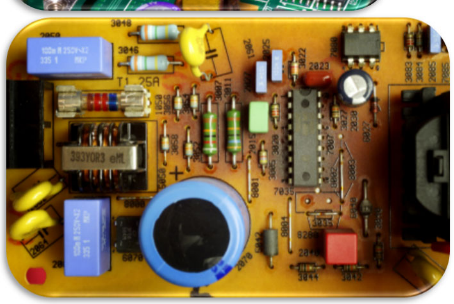
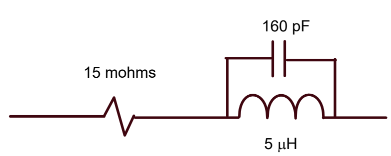
Inductors Have Resistance and Capacitance









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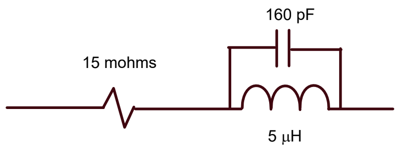
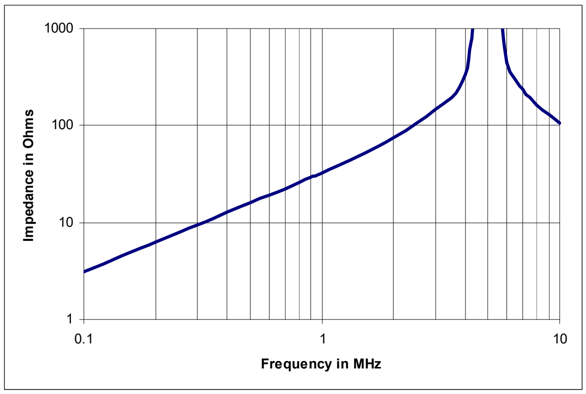
Impedance of a 5-μH Inductor





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Types of Inductors

- **Ferrite Core**
  High inductance in small package
- **Air Core**
  Linear behavior under high-current conditions
- **Common-mode**
  Impedes common-mode currents while passing differential-mode currents.

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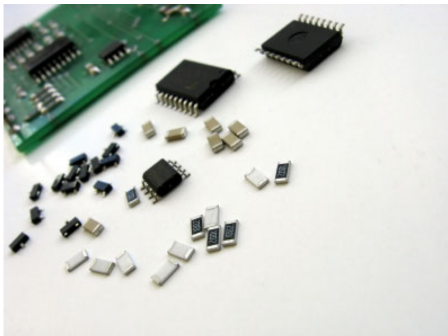
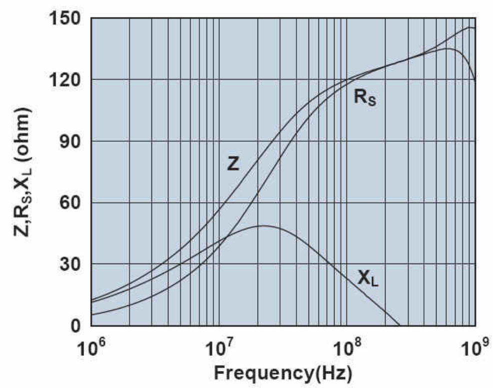
Ferrites



Fair-Rite 2643000701



Estimating Parasitic Values

Resistance of a circuit board trace:

Resistance per meter of a wire:

Capacitance of a ping pong ball:

Capacitance of a person:

Self capacitance of a heatsink:

Capacitance between planes of a circuit board:

Inductance of a 10-cm diameter wire loop:

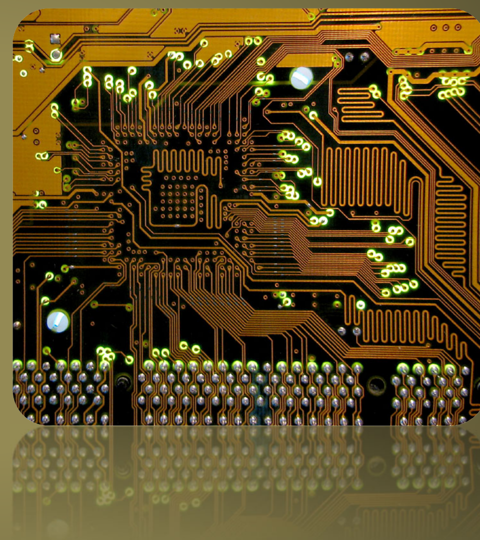
Inductance per cm of a ground strap or pigtail:

Inductance per cm of a microstrip circuit board trace:

Connection inductance of an SMT component on a circuit board:

Electromagnetic Compatibility Principles and Design

Signal Routing and Termination



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Ground vs. Current Return

An Important Point

Grounding and Current Return are two VERY different functions!

- A grounding conductor connects two points in a system in a manner that ensures they have the same voltage.
- A current return conductor provides a path for power or signal currents to return to their source.
- In most cases, these are incompatible functions. Grounding conductors should never carry intentional power or signal currents.

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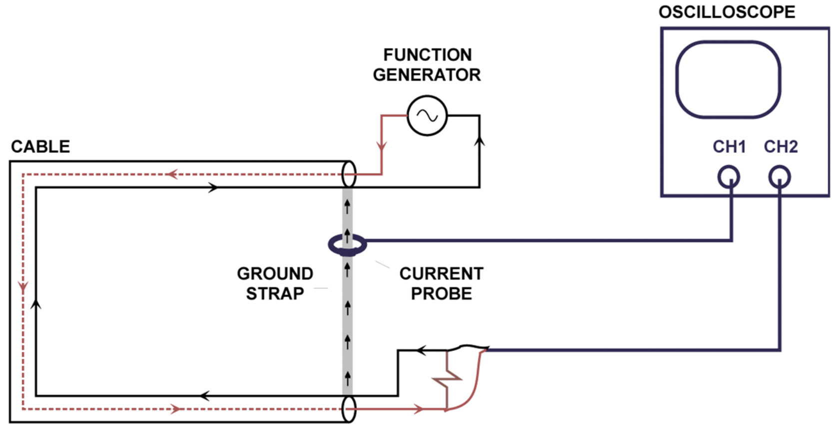
Identify Current Paths

Where does the return current flow?



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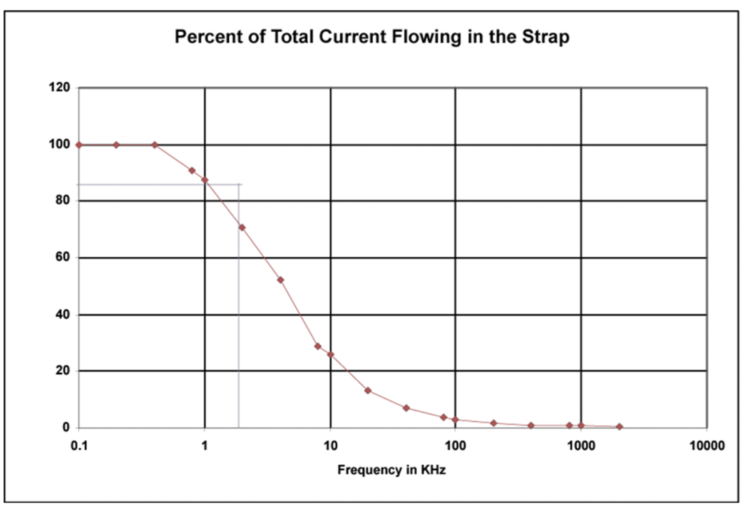
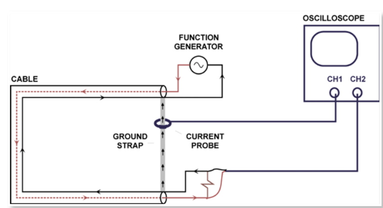
Identify Current Paths





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Identify Current Paths

Current takes the path of least impedance!

> 100 kHz this is generally the path of **least inductance**

< 10 kHz this is generally the path(**s**) of **least resistance**

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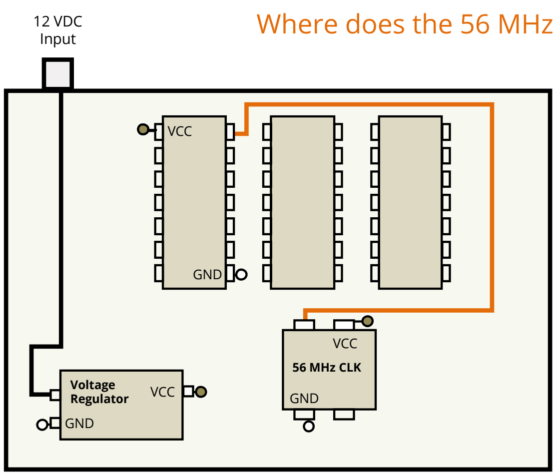
Identify Current Paths

Where does the 56 MHz return current flow?



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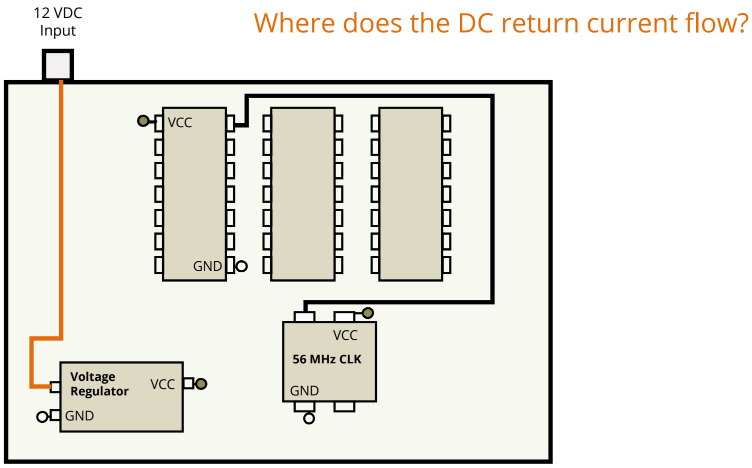
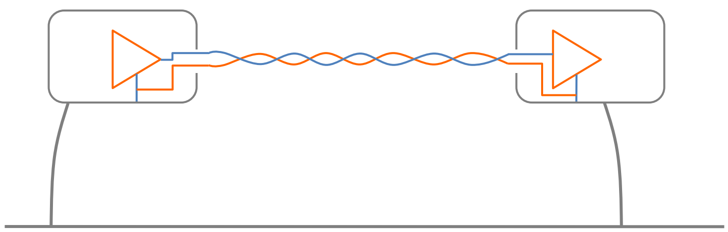
Identify Current Paths



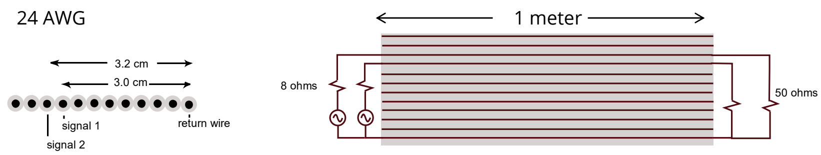
Identify Current Paths

Where does the return current flow?



Identify Current Paths

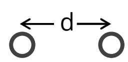
Where does the 10 MHz return current flow?



Parallel Wires

$$L = \frac{\mu}{\pi}\cosh^{-1}\left(\frac{d}{2a}\right)$$

wire radius: a



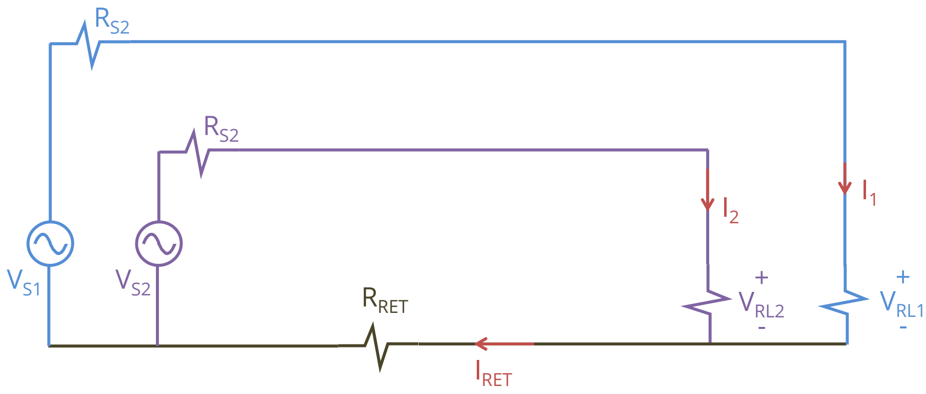
At 10 MHz: $L = 1.93\ \mu H$

$\omega L = 121\ \Omega$

Key Points

- Above 1 MHz, all we have to do is provide a good low-inductance return paths for all signals and the currents will take those paths.
- Below 100 kHz, might have to maintain control of current return path with an isolated return. Do a calculation to ensure that it is necessary before isolating return paths.

Calculation of Common-Impedance Coupling



We can solve this circuit using SPICE or loop and node equations, but that takes time and inhibits an intuitive understanding for what is really happening.

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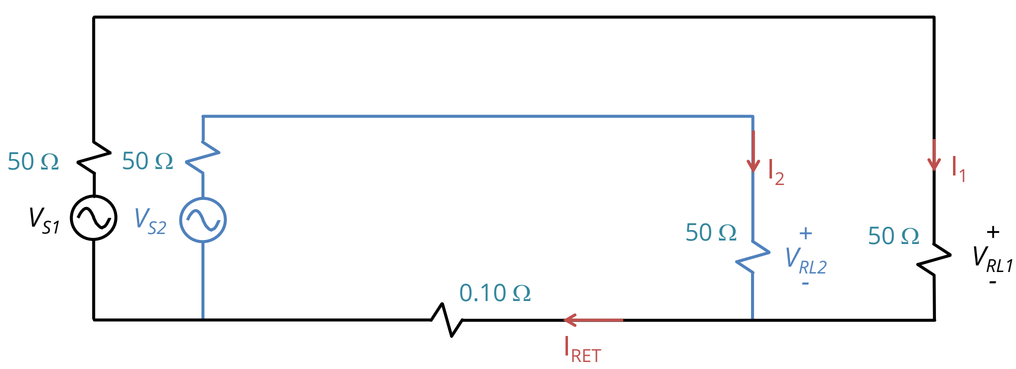
Calculation of Common-Impedance Coupling



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Quantifying Common-Impedance Coupling

Maximum common impedance coupling is easy to quantify!

$$\underset{\text{(worst-case)}}{V_{coupled}} = \underset{\text{(worst-case)}}{I_{source}} \times \underset{\text{(worst-case)}}{R_{shared}}$$

- Perform this calculation when you suspect conducted coupling will be an issue.
- ALWAYS perform this calculation before isolating signal returns labeled “ground”!

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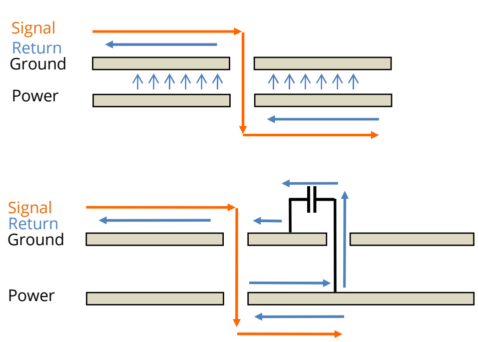
Current paths in traces that pass between plane pairs



Closely Spaced Planes
(e.g.; < 10 mils or 0.25 mm)

Widely Spaced Planes
(e.g.; > 20 mils or 0.5 mm)

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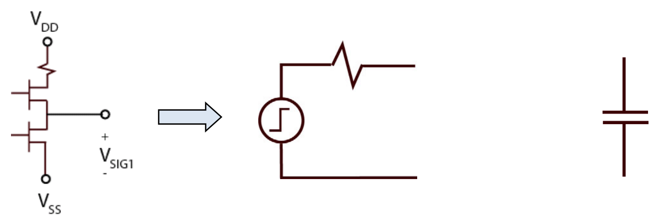
Signal Termination

CMOS Driver Model

CMOS Input Model



Signal Transition Times

OBSOLETE

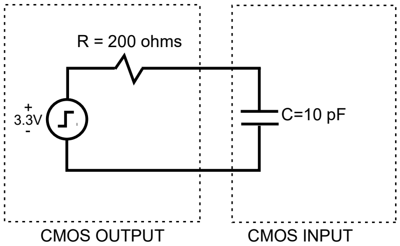
Device Switching Times

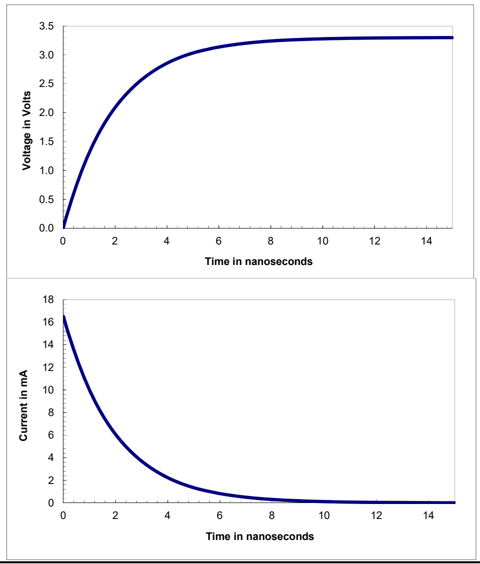
DEVICE TYPE	RISETIME
Standard TTL	5.0 ns
Schottky TTL	3.0 ns
ASTTL	1.9 ns
[illegible]TTL	1.2 ns
BiCMOS	0.7 ns
[illegible]0KH ECL	0.7 ns
100K ECL	0.5 ns
GaAs	0.3 ns

Actual transition times are usually slower and are determined by the external connections and loads.

For capacitive loads: $t_r \approx 2.2RC$

Step Response of an RC Circuit

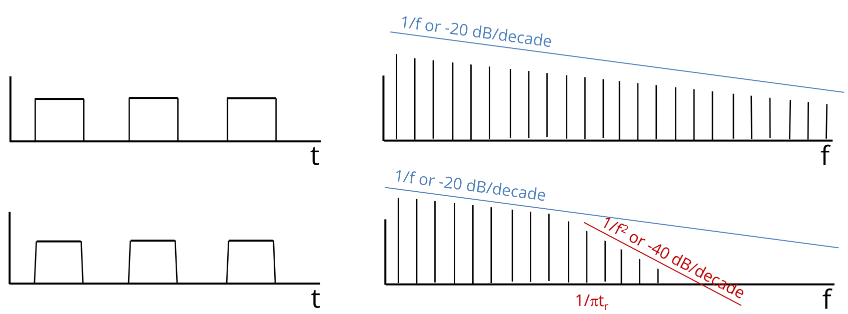




Capacitors initially look like a short circuit, and eventually look like an open circuit.

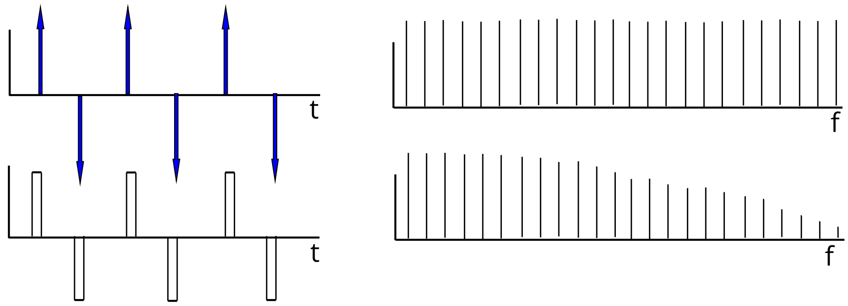
$t_r \simeq 2.2RC$

Signal Voltage



Control transition times of digital signals!

Signal Current



Control transition times of digital signals!

Can use a series resistor when load is capacitive.

Use appropriate logic for fast signals with matched loads.

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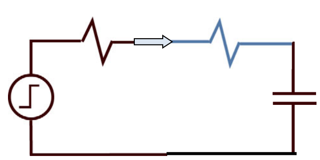
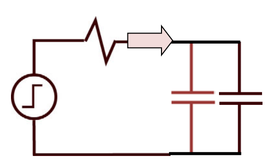
Signal Termination

Reducing risetime with a series resistor



Good idea!

Reducing risetime with a parallel capacitor



Bad idea!

High-Frequency currents are not reduced.

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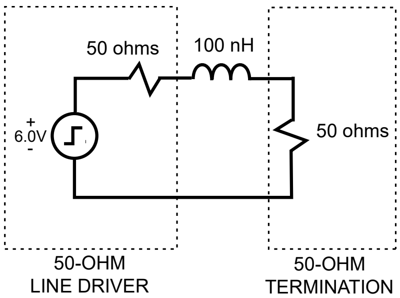
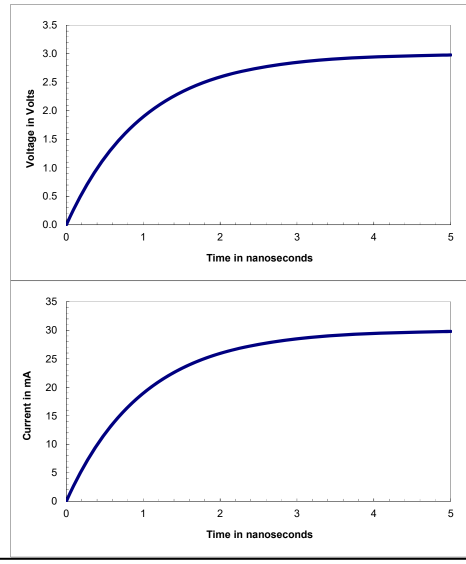
Step Response of an RL Circuit



Inductors initially look like an open circuit and eventually look like a short circuit.

$$t_r \simeq 2.2\, L/R$$



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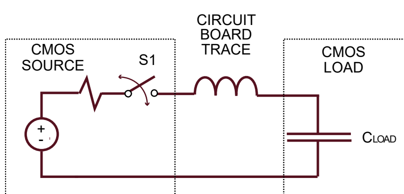
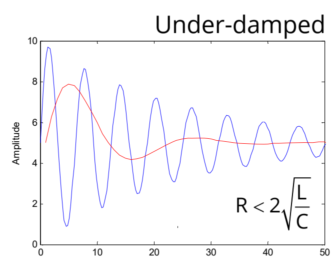
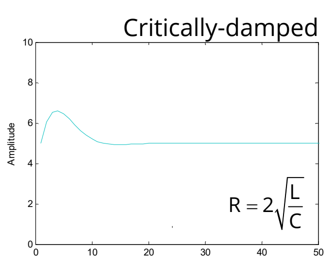
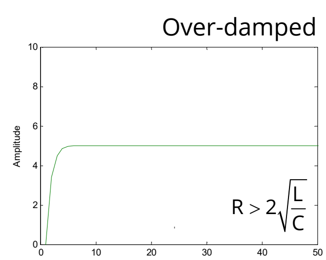
Series RLC Circuit Response









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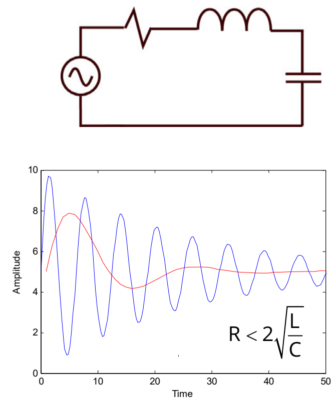
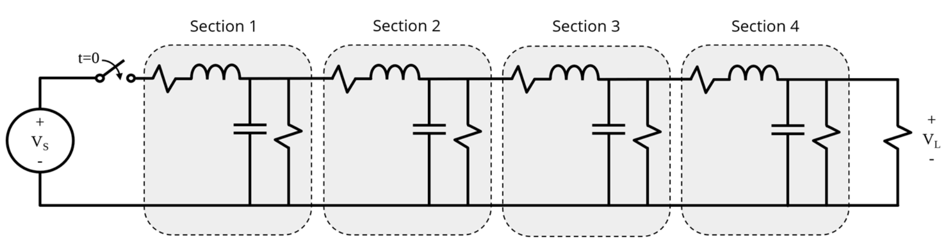
Eliminate LC Ringing with a Series Resistor

IF you have ringing due to a series LC resonance:



- Reduce the inductance
- Increase the capacitance
- Add a resistance (ferrite?)
- Value should be …

RLCG Parameters



If the length of each section of the RLCG lumped model is small relative to a wavelength (e.g., $\ell_n \ll \lambda/8$), the electrical behavior of the model is the same as the electrical behavior of the transmission line.

Propagation Velocity

Determined by the dielectric material

Propagation velocity (m/sec)

$$v = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{\mu\varepsilon}}$$

Inductance per unit length (H/m)

Capacitance per unit length (F/m)

This term is independent of the geometry

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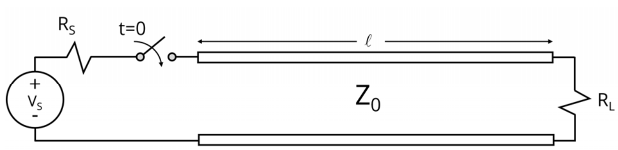
Propagation Delay (Electrical Length)



$$t_{PD} = \frac{\ell}{v}$$

Propagation Delay (sec)

The propagation delay is the amount of time required for a signal to propagate from one point to another point (total distance, ℓ) on the transmission line.

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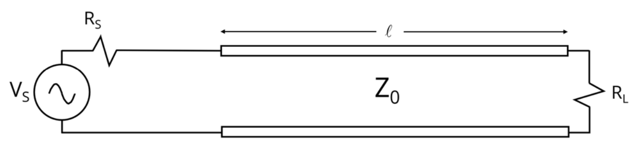
Characteristic Impedance



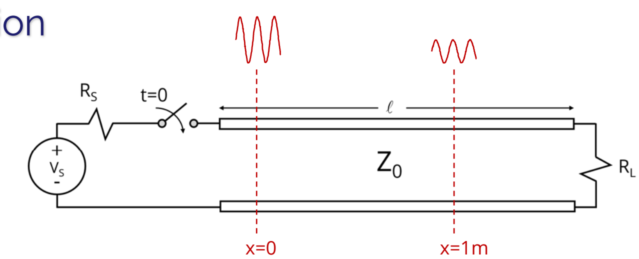
$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \approx \sqrt{\frac{L}{C}}$$

Characteristic Impedance (ohms)

Low-Loss Approximation

The characteristic impedance is the ratio of the voltage to the current in a signal traveling in one direction down the transmission line.

Attenuation



$$V = V_0 e^{-\gamma x}$$

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta$$

$$\text{Attenuation in dB/m } = 20\log\left(\frac{V_0 e^{\alpha(x=0m)}}{V_0 e^{\alpha(x=1m)}}\right) = 20\log\left(e^{-\alpha}\right) = 8.7\alpha$$

$$\alpha \approx \frac{R}{2Z_0} \qquad \beta \approx \omega\sqrt{LC}$$

Low-Loss Approximation

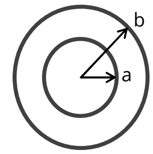
$$\text{Attenuation in dB/m} \approx \frac{4.34R}{Z_0}$$

Examples

RG58 Coaxial Cable

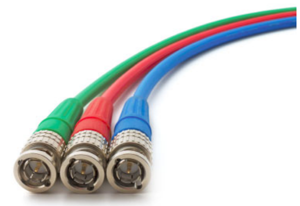
Coaxial Cable

$$L = \frac{\mu}{2\pi}\ln\left(b/a\right)$$



Outer conductor diameter:	4.2 mm
Inner conductor diameter:	1.2 mm
Dielectric permittivity:	2.3

Propagation Delay:	5.0 nsec/m
Characteristic Impedance:	50 Ω
Capacitance per unit length:	100 pF/m
Inductance per unit length:	250 nH/m
Resistance per unit length (1 MHz):	90 mΩ/m
Cable Attenuation at 1 MHz:	7.8 dB/km



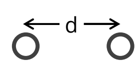
Coaxial cables typically have characteristic impedances between 20 and 90 ohms.

Examples

CAT5e TWP

Parallel Wires

$$L = \frac{\mu}{\pi}\cosh^{-1}\left(d/2a\right)$$



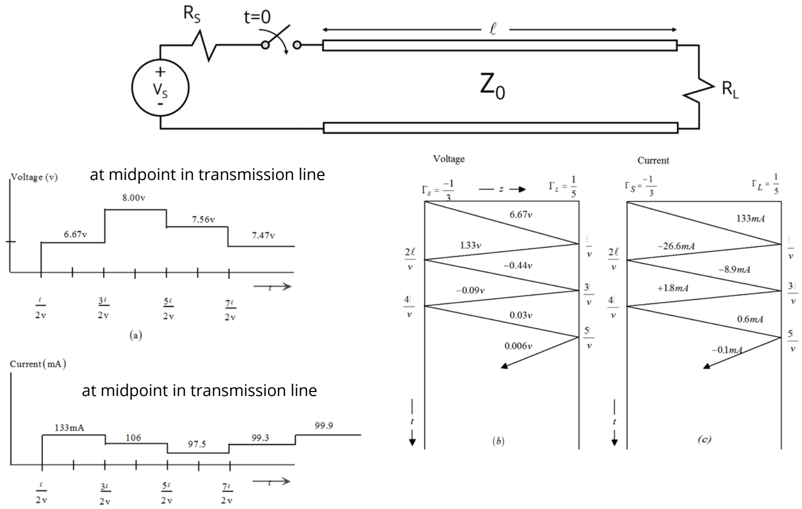
wire radius: a

Conductor diameter:	0.511 mm
Conductor separation:	1.0 mm
Dielectric permittivity:	2.4

Propagation Delay:	5.2 nsec/m
Characteristic Impedance:	100 Ω
Capacitance per unit length:	52 pF/m
Inductance per unit length:	520 nH/m
Resistance per unit length (1 MHz):	327 mΩ/m
Cable Attenuation at 1 MHz:	14 dB/km

Wire pair cables typically have characteristic impedances between 100 and 300 ohms.

When is a cable or trace a transmission line?



Technically, always! But it will be most important to us when the propagation delay is greater than the transition time.

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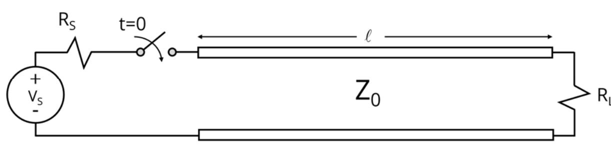
When must a cable be modeled as a transmission line?



The answer depends on the application, but generally the following guidelines apply.

For digital signals: When $t_r < 2 * t_{pd}$

For RF signals: When $\ell > \lambda/8$

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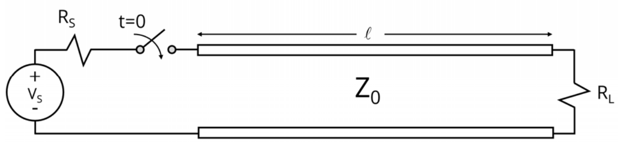
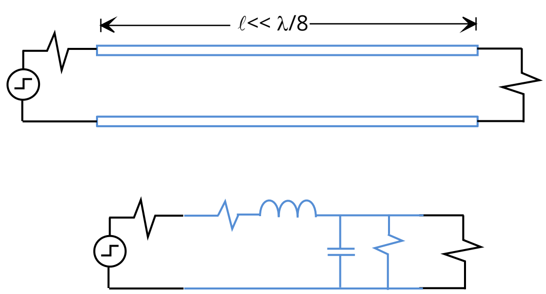
An Important Point



In most applications, anything that must be modeled as a transmission line must have a matched termination. This is usually undesirable from a cost and EMC perspective. Therefore, every effort should usually be taken to ensure that the signal bandwidth is no higher (or transition times are no shorter) than necessary.

When cables are electrically short …

- They can be modeled using their lumped RLCG parameters.



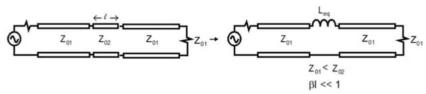
- Often, one or none of these parameters is significant relative to the source and load impedances.

When cables are electrically short …

When connection discontinuities are electrically short …

Be careful not to model short cables or connectors with the full L or C unless you have shown the that other parameter can be neglected.

Discontinuities with a characteristic impedance greater than the source and load impedances can be modeled with a lumped inductance.



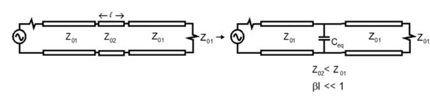
The value of this inductance is less than the value of the lumped parameter L in the RLCG model.

$$L_{eq} \approx L\ell\left[1-\left(\frac{R_{01}}{Z_{02}}\right)^2\right]$$

When connection discontinuities are electrically short …

Be careful not to model short cables or connectors with the full L or C unless you have shown the that other parameter can be neglected.

Discontinuities with a characteristic impedance less than the source and load impedances can be modeled with a lumped capacitance.



The value of this capacitance is less than the value of the lumped parameter C in the RLCG model.

$$C_{eq} \approx C\ell\left[1-\left(\frac{Z_{02}}{R_{01}}\right)^2\right]$$

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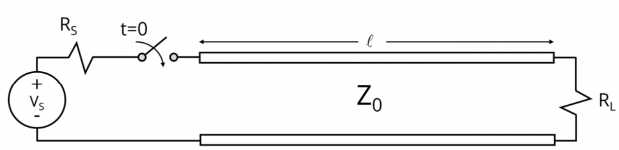
When cables are not electrically short …

To eliminate reflections, transmission lines <u>that are not electrically short</u> must have a controlled impedance and must be matched!



- For signals with one source and one load, the match can occur at the source end: **$R_S = Z_0$**.
- For signals with one source and more than one load, the match must generally occur at the load end: **$R_L = Z_0$**.

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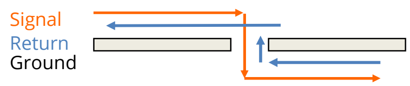
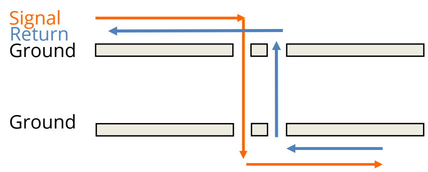
When Routing Controlled Impedance Traces

- When routing a trace between layers, route on either side of the same return plane.



- When routing a trace between 2 different planes, use a transfer via near the signal via.



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Key Points

- All signal paths with a propagation delay greater than the signal transition time should be treated as transmission lines (i.e.; have a controlled impedance and a matched source and/or load).
- Control ALL transition times on the board so that only the longest and fastest signal paths need to be matched.
- On most well-designed boards, the percentage of traces with controlled impedances is nearly zero, while the percentage of traces with controlled transitions times is very high.

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Remember!

- **Don't use matched terminations and controlled impedance traces unless you are forced to!**
  - by a signal specification (e.g.; CAN, USB, HDMI)
  - by need to send very high-speed signals long distances (e.g.; 100 Mbps > 10 cm)
- Instead, control ALL transition times so that $t_r > 2 * t_{pd}$.

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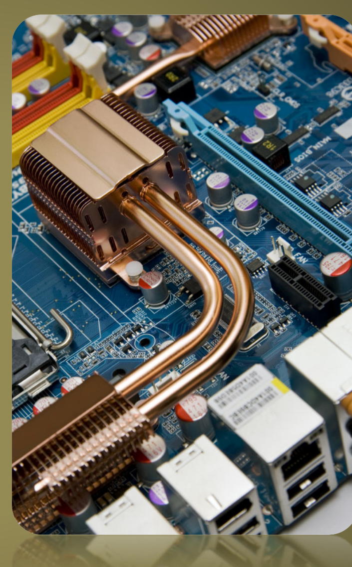
Electromagnetic Compatibility Principles and Design

Identifying Unintentional Antennas



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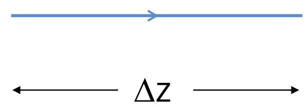
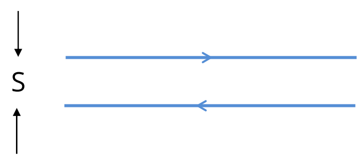
Common-Mode vs. Differential-Mode Radiation



$$E_{max} = 0.63 \times 10^{-6} \frac{|I_c| f \Delta z}{r}$$



$$E_{max} = 1.32 \times 10^{-14} \frac{|I_d| f^2 s \Delta z}{r}$$

$$= 0.63 \times 10^{-6} \frac{|I_d| f \Delta z}{r} \left(2\pi \frac{s}{\lambda} \right)$$

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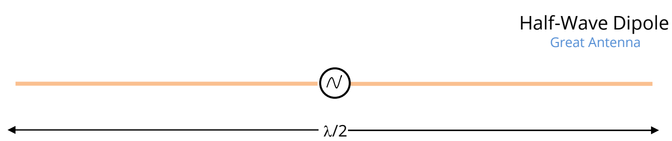
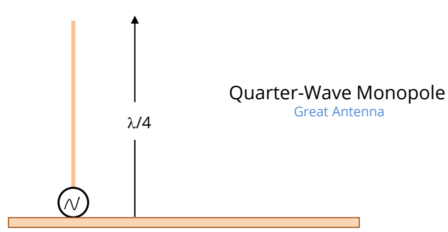
Identifying Antennas

What makes an efficient antenna?





Requirements for a great antenna

1. size
2. two halves

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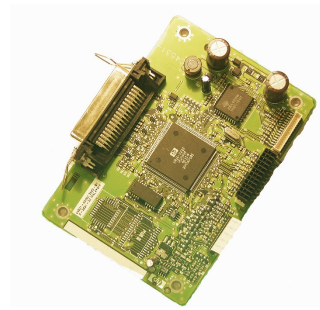
Identifying Antennas

Good Antenna Parts		Poor Antenna Parts	
<100 MHz	>100 MHz	<100 MHz	>100 MHz
Cables Metal Chassis or Enclosure	Tall Components or Heatsinks Seams in shielding enclosures Sparsely populated power planes	Microstrip or stripline traces Anything that is not big	Integrated Circuits Microstrip or stripline traces



Free-space wavelength at 100 MHz is 3 meters

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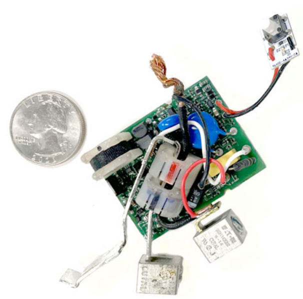
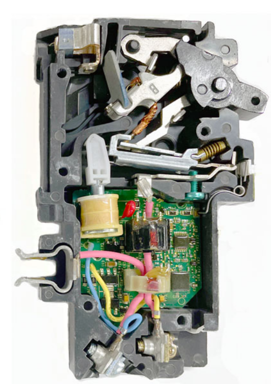
Identifying the Antennas/Ports

Where are the antennas on these boards?





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Key Points

- Efficient EM radiation requires an antenna with 2 halves driven by a voltage.
- Efficient antenna halves are big enough to easily identify. They are generally on the order of a tenth to a quarter of a wavelength in size or larger.

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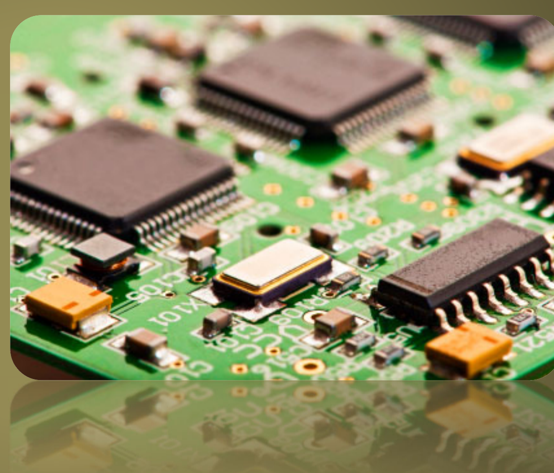
Electromagnetic Compatibility Principles and Design

Noise Sources and Coupling Mechanisms



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Identifying Sources (Diagnostics)

Clocks	Narrow band, consistent
Digital Data	Not as narrow as clocks, but clock frequency is usually identifiable.
Analog signals	Bandwidth determined by signal source, consistent
Power supply switching	Appears broadband, but harmonics of switching frequency can be identified, consistent

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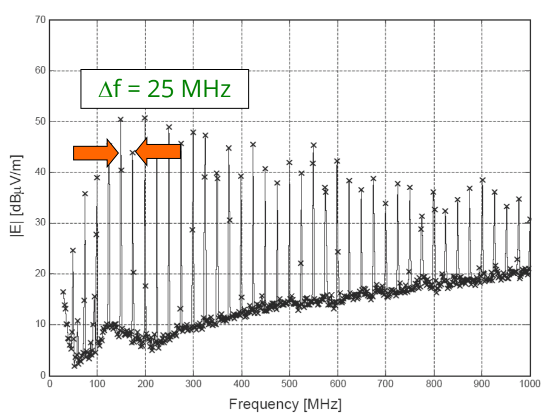
Identifying Sources (Diagnostics)

What is the source clock frequency?



Radiation from a circuit board with an attached cable

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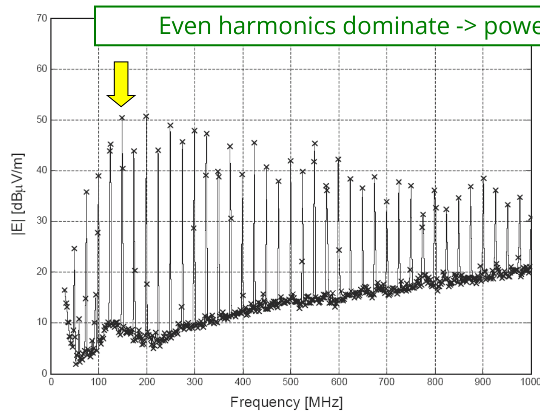
Identifying Sources (Diagnostics)

Power or signal source?



Radiation from a circuit board with an attached cable

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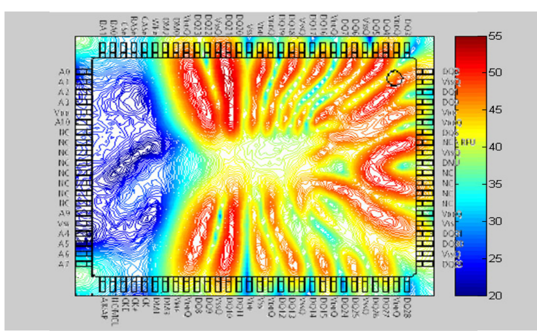
Identifying Sources

Active Devices (Power Pins)



For some ICs, the high-frequency currents drawn from the power pins can be much greater than the high-frequency currents in the signals!

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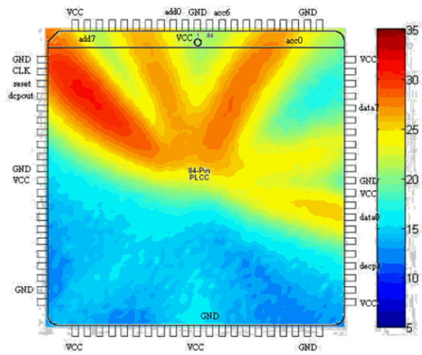
Identifying Sources

Noise on the low-speed I/O



For some ICs, significant high-frequency currents appear on low-speed I/O including outputs that never change state during normal operation!

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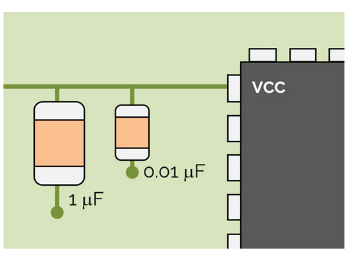
Parasitic Oscillations



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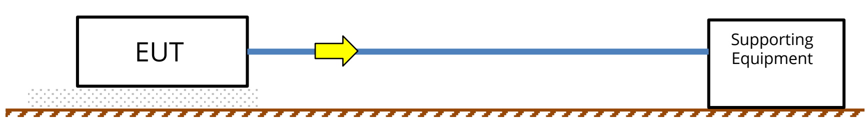
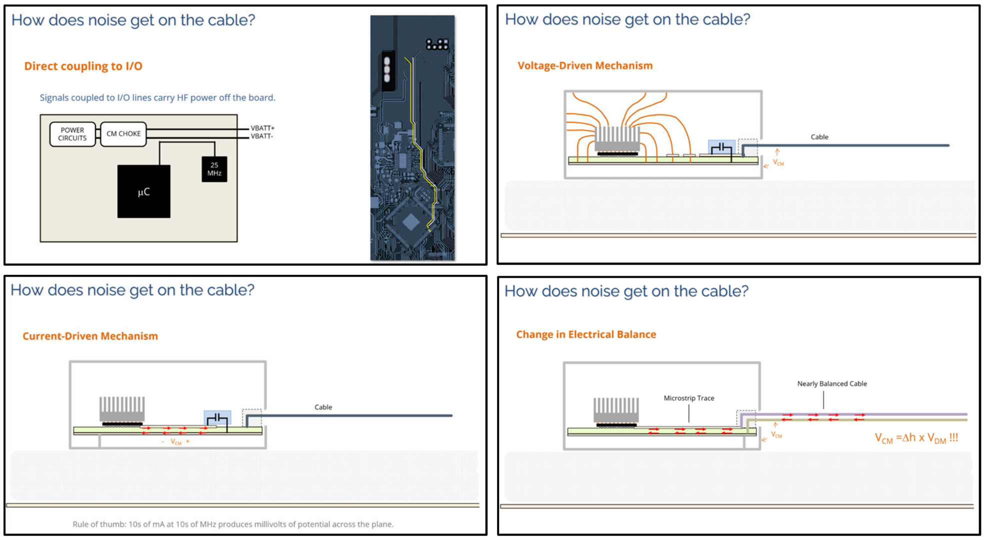
Key Points

- ALL pins of an active device can be significant sources of high-frequency current if the device is switching internally at high frequencies. Don't assume a nominally low-speed trace doesn't have high-frequency currents flowing on it.
- Relatively weak sources can be enhanced by parasitic resonances.

Coupling between unintentional sources and antennas



Problems that cause nearly all radiated emissions < 500 MHz



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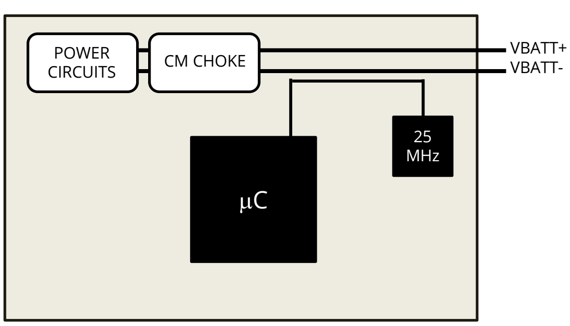
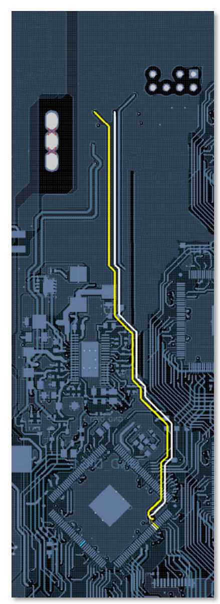
How does the component drive the cables?

Direct coupling to I/O

Signals coupled to I/O lines carry HF power off the board.





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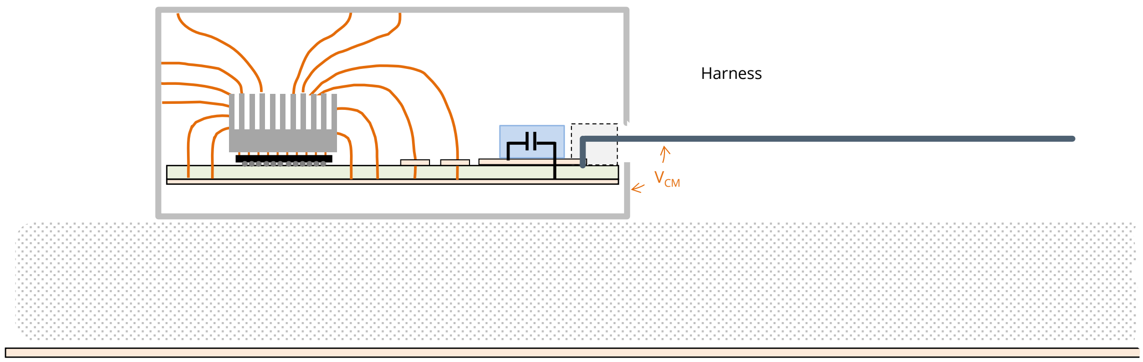
How does the component drive the harness?

Voltage-Driven Mechanism



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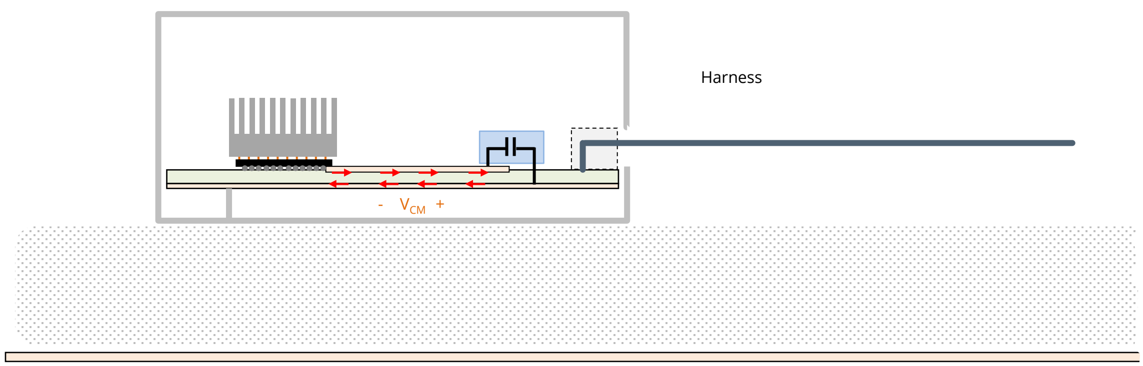
How does the component drive the harness?

Current-Driven Mechanism



Rule of thumb: 10s of mA at 10s of MHz produces millivolts of potential across the plane.

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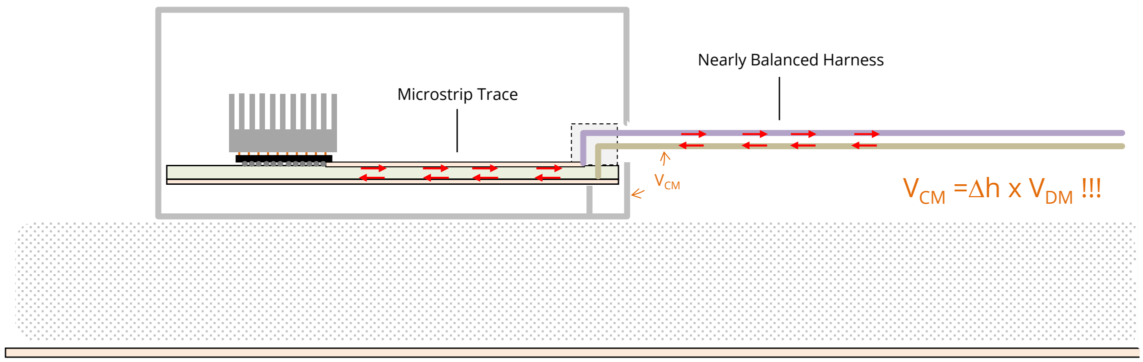
How does the component drive the harness?

Change in Electrical Balance



Rule of thumb: 10s of mA at 10s of MHz produces millivolts of potential across the plane.

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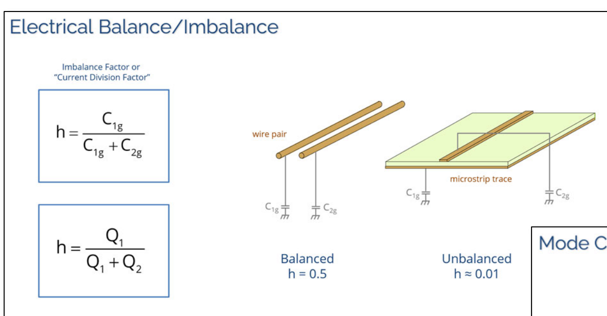
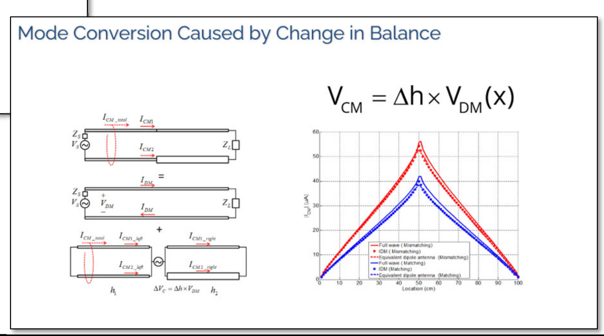
Electrical Balance



Single-ended sources should use unbalanced transmission lines and unbalanced terminations!



Differential sources should use balanced transmission lines and balanced terminations!

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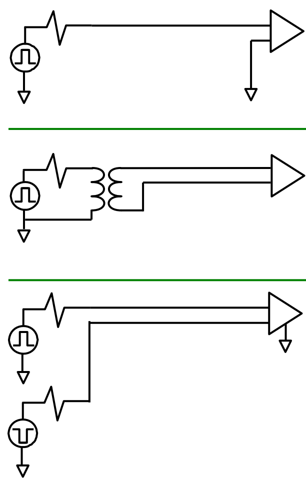
Single-ended vs. Differential Signaling



Single-ended
- Unbalanced
- Currents return on "ground"
- Requires N+1 conductors
- Inexpensive parts

Differential
- Balanced
- No signal current on ground
- Requires 2N conductors
- Requires balun

Pseudo-Differential
- Nominally Balanced
- Nominally no HF current on ground
- Always has a CM voltage component!!
- Requires 2N conductors
- No balun required

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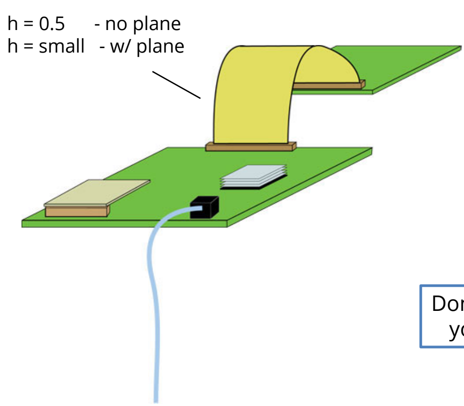
Driving a Ribbon Cable



- A perfect differential driver driving two adjacent wires in a ribbon cable produces no common-mode current on the ribbon cable.
- A single-ended driver driving two adjacent wires in a ribbon cable produces exactly the same amount of common-mode current as a common-mode source with half the signal voltage

Don't drive ribbon cable wires with single-ended sources unless you know the common-mode current will not be a problem.

Single-ended sources should use unbalanced transmission lines and unbalanced terminations!

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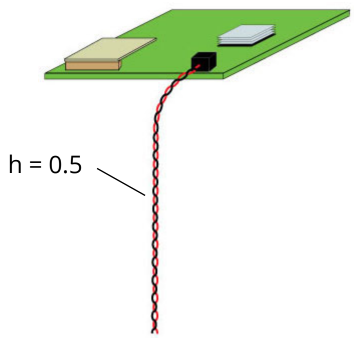
PCB Driving a Twisted Wire Pair



- A perfect differential driver driving a perfect twisted-wire pair produces no common-mode current on the wire pair.
- A single-ended driver driving a twisted-wire pair produces exactly the same amount of common-mode current as a common-mode source with half the signal voltage

Don't drive twisted-wire pairs with single-ended sources unless you know the common-mode current will not be a problem.

Differential sources should use balanced transmission lines and balanced terminations!

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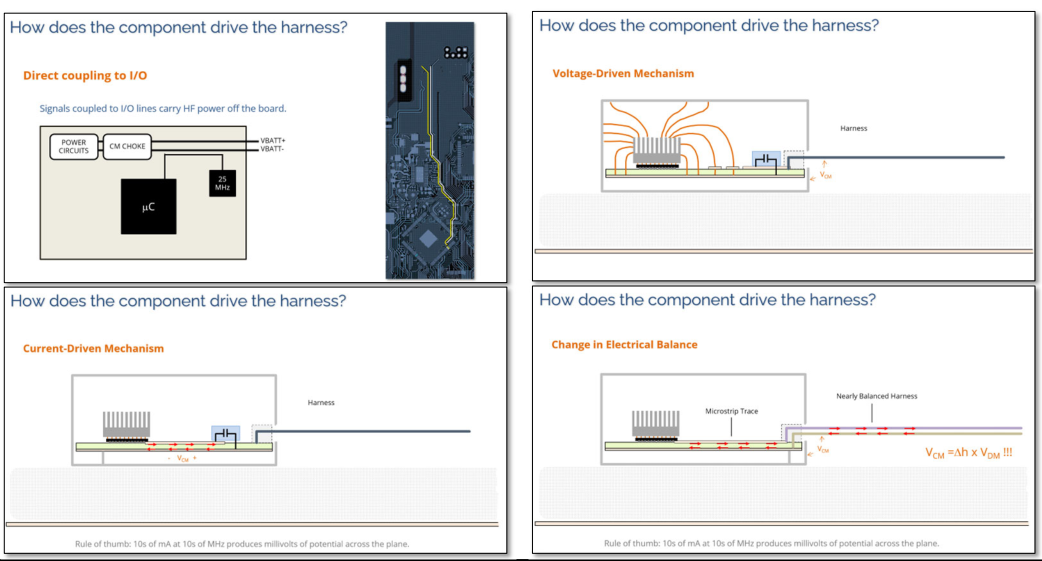
Problems that cause nearly all component-level emissions



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What about frequencies above a few hundred MHz?

- Cables are much less likely to be the antenna.
- Most common GHz antenna on a PCB is lightly loaded planes.
  - Ground planes should be stitched together frequently.
  - Power planes should be close to ground planes (e.g., < 0.25 mm)
  - Power planes should have lots of connections (active devices and decoupling capacitors)
  - Don't extend power planes to areas of the board where they are not used, and don't allow one section of power plane to become choked off from another section.
- Avoid having large-valued ceramic capacitors connected to the same power/ground plane pairs as small-valued ceramic capacitors. They will support a parasitic oscillation typically at GHz frequencies.

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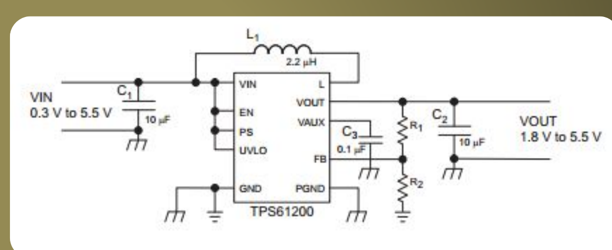
Electromagnetic Compatibility Principles and Design

Grounding



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Things Labeled Ground

- Safety / Lightning Protection Conductors
- EMC Ground Structures
- Power ~~and Signal Current~~ Returns

Current return is generally incompatible with grounding!!!

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Definition of Ground

ANSI C63.14 - 1992 Dictionary for Technologies of Electromagnetic Compatibility

4.151 - Ground, F
The electrically int … nt paths
to earth. The facili … , signal
reference subsyst … ets,
conduit, junction b … ts.
4.152 - Grounding
(1) The bonding of … mon
potential.
(2) The connecting … e extent
that serves in plac

Ground is a conductor that serves as a reference potential and <u>does not carry current</u>!

National Electrical Code
Ground
A conducting connection, whether intentional or accidental, between an electrical circuit or equipment and the earth or to some conducting body that serves in place of the earth.

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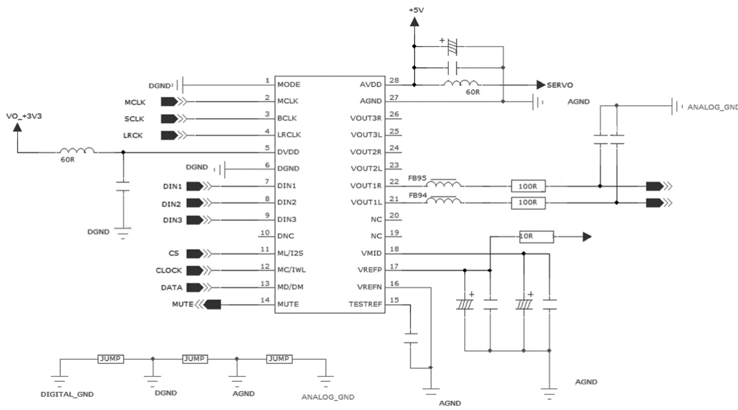
What is “ground”?



Why are there 4 different grounds in this circuit?

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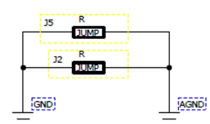
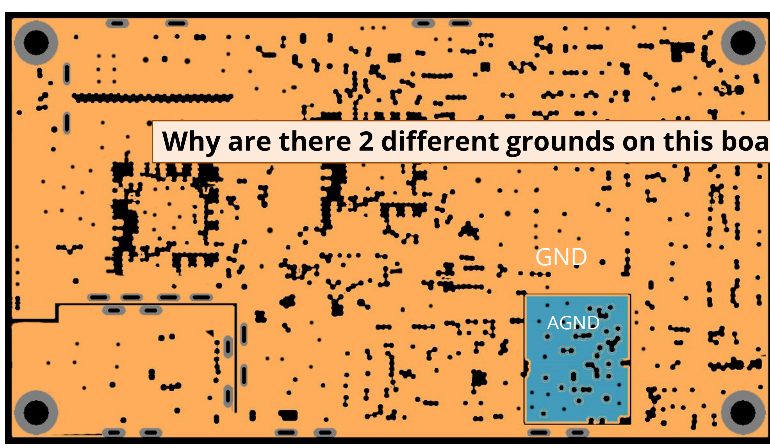
What is “ground”?





Why are there 2 different grounds on this board?

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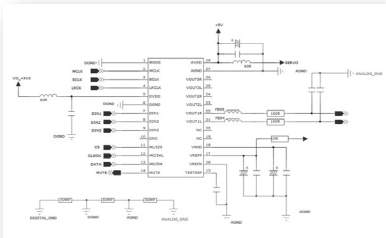
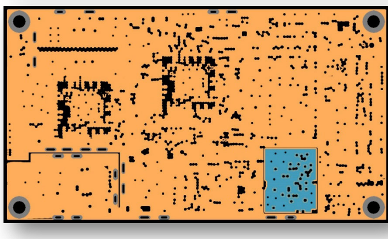
What is "ground"?





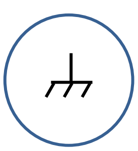
These are not grounds!

They are current return conductors!

They are isolated to prevent Common-Impedance Coupling!

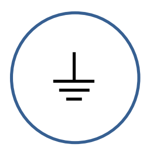
Grounding is not the same as current return!

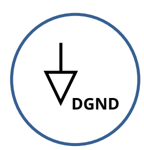
Ground vs. Signal Return



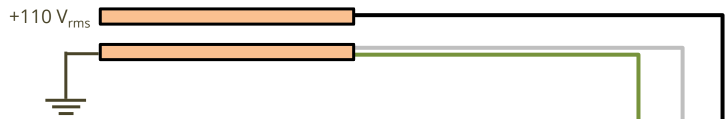
"Whenever I see more than one of these symbols on the schematic, I know there is [EMC] work for us here."

T. Van Doren





Safety Ground



Ground is <u>NOT</u> a Current Return Path

The purpose of a system ground is to provide a <u>reference voltage</u> and/or a safe path for <u>fault</u> currents.

In order to serve this function, a ground conductor cannot carry any “objectionable” current.

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Ground Conductors vs. Signal Return

The purpose of a system ground is to provide a reference voltage and/or a safe path for <u>**fault**</u> currents.

Signal or power currents flowing on a “ground” conductor can prevent a ground conductor from serving its intended purpose.

<u>**Don’t confuse ground conductors with signal return conductors.**</u> Rules for the routing of “ground” may conflict with the rules for routing signal or power returns.

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EMC Ground Structure

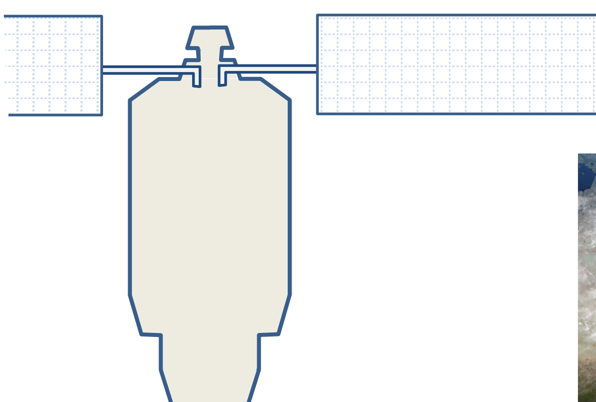
A ground structure doesn't need to be electrically small to be effective.
However, it is important not to induce a voltage between any two parts of the ground structure.

EMC Ground Structures

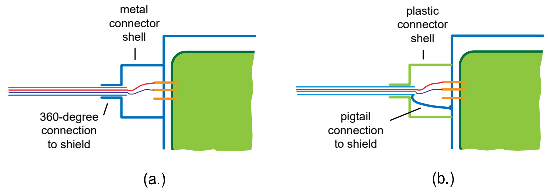
- Are good conductors
- May be electrically large
- Do not carry intentional signal currents

EMC Ground Structures

A ground structure doesn't need to be electrically small to be effective.
However, it is important not to induce a voltage between any two parts of the ground structure.



Grounding Conductors



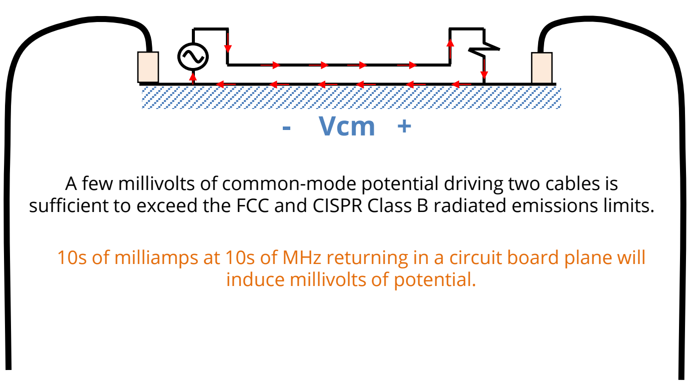
Grounding Conductors

- Are good conductors
- Have low inductance as well as low resistance
- May **NOT** be electrically large
- Do not carry intentional signal currents

Is a "ground plane" a ground structure?

Current Driven Radiation Mechanism

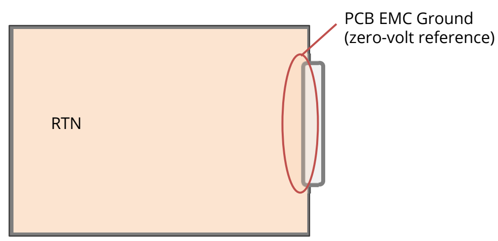
Signal current loop induces a voltage between two good antenna parts.



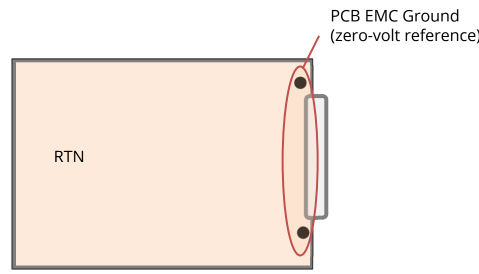
A few millivolts of common-mode potential driving two cables is sufficient to exceed the FCC and CISPR Class B radiated emissions limits.

10s of milliamps at 10s of MHz returning in a circuit board plane will induce millivolts of potential.

Where is the Circuit Board Ground?



PCB in product with no ground structure



PCB mounted near the ground structure

PCB ground cannot be at a different potential than the ground structure.

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If DC Isolation is Required

Lateral Isolation
Can we guarantee that each attached cable is within 1 mV of the ground structure at radiated emissions frequencies?

Vertical Isolation
Provides low-frequency isolation, while facilitating high-frequency bonding.

- All planes that reference signals that leave the board should be tied to ground with capacitors.
- Only one plane usually needs to be full size.
- One or zero vias should connect planes with different labels.

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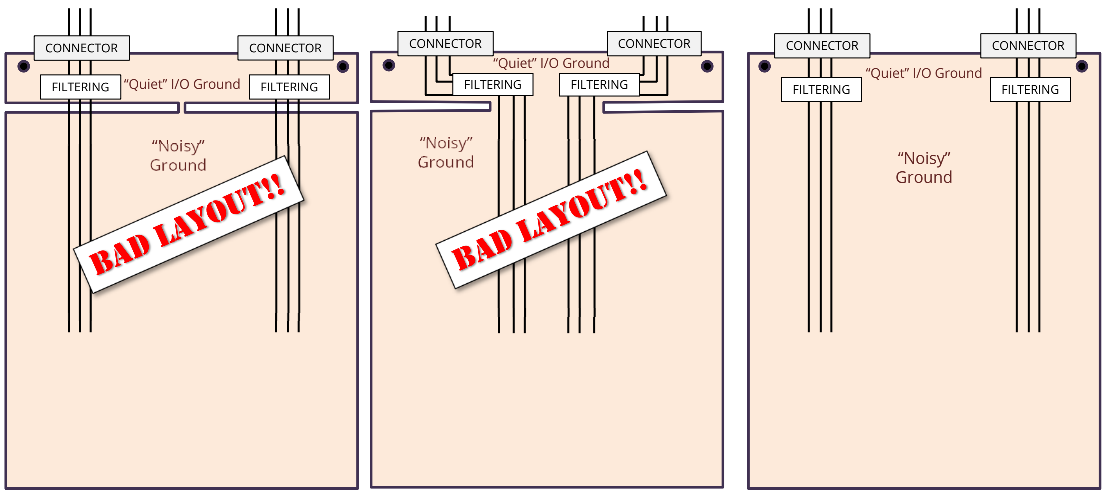
Two Bad Ground Plane Layouts (and one good one)



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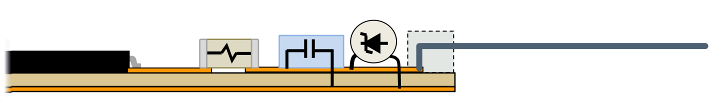
To meet EMC requirements …

Boards on or near metal structure:

- Connect to it! Those connections are your board grounds.
- **Either** Bond (at RF) everything that leaves the board or is electrically large to those grounds,
- **Or** control transition times and essentially filter everything.

Boards far from any metal structure:

- Designate your board ground (0-V reference) near external connector edge.
- **Either** bond (at RF) everything that leaves the board or is electrically large to that ground,
- **Or** control transition times and essentially filter everything.



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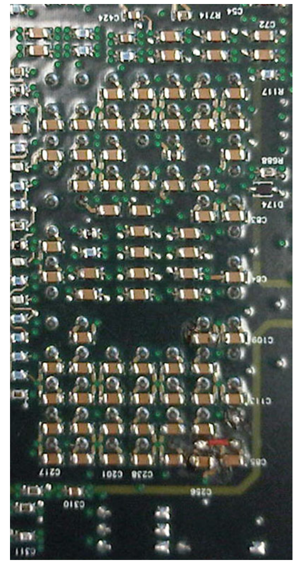
Capacitors from I/O to Chassis

Caps on every connector pin

Better implementation



Rules for Grounding

- Designate one location or one non-current-carrying metal structure as your zero-volt reference or ground.
- Be sure that all other metal structures including attached cables and large heatsinks do not deviate from the ground potential by more than an acceptable limit.
- For radiated emissions (10s of MHz and higher), this acceptable limit is on the order of 1 mV.
- For safety, the acceptable limit is generally on the order of 10s of volts.

To meet EMC requirements …

Boards on or near metal structure:

- Connect to it! That connection is your board ground.
- Bond (at RF) everything that leaves the board or is electrically large to that ground.

Most medium to large printed circuit boards.

Boards far from any metal structure:

- Designate your board ground (0-V reference).
- **Either** bond (at RF) everything that leaves the board or is electrically large to that ground
- **Or** control transition times and essentially filter everything.

Many sensors and actuators

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Ground is NOT Current Return!

Rules for Grounding

- Designate one location or one non-current-carrying metal structure as your zero-volt reference or ground.
- Be sure that all other metal structures including attached cables and large heatsinks do not deviate from the ground potential by more than an acceptable limit.
- For radiated emissions (10s of MHz and higher), this acceptable limit is on the order of 1 mV.
- For safety, the acceptable limit is generally on the order of 10s of volts.

Rules for Current Return Routing

- At frequencies below 1 MHz, provide a low-resistance current return path. Be aware of alternate return paths and the possible consequences.
- At frequencies below 1 MHz, if sharing a return conductor will cause unacceptable common-impedance coupling, then don't share the return conductor.
- At frequencies above 1 MHz, provide a low-inductance current return path. Watch for field-coupling to other circuits and structures that could result in significant conductor or radiated emissions.

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Summary of Key Points

- Grounding is a critical aspect of EMC and product safety.
- Grounding is all about providing a reference potential.
- Grounding is **NOT** about returning currents to their source.
  - Unfortunately, many current return nets in circuits are labeled ground, and
  - Paying attention to current return paths is also an important aspect of meeting EMC and signal integrity requirements.
- Identifying and maintaining the integrity of a **grounding structure** is an important part of designing for EMC and product safety.

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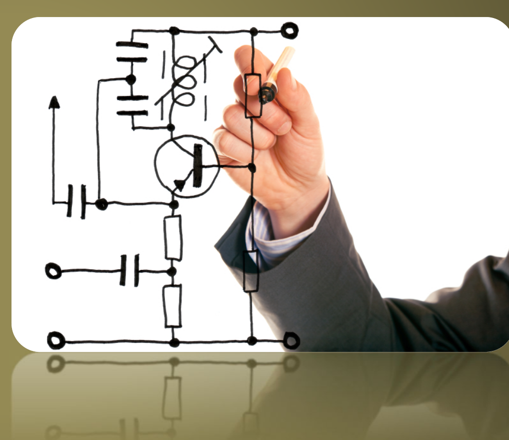
Electromagnetic Compatibility Principles and Design

"Ground" in Mixed-Signal Environments



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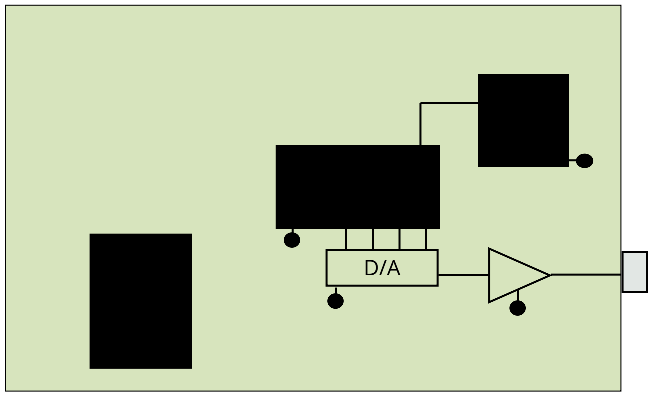
Ground vs. Signal Return

Exercise: Trace the path of the digital and analog return currents.



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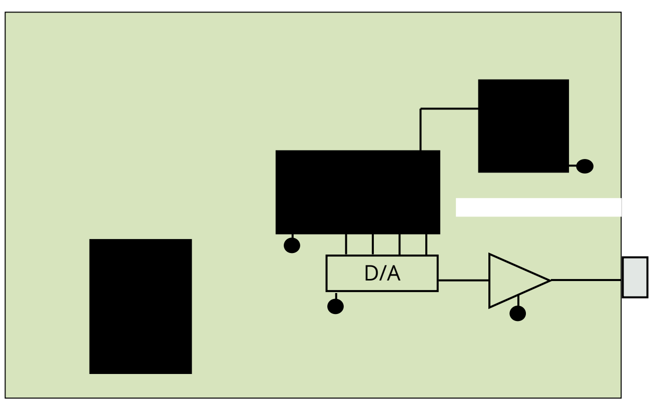
Ground vs. Signal Return

Exercise: Trace the path of the digital and analog return currents.



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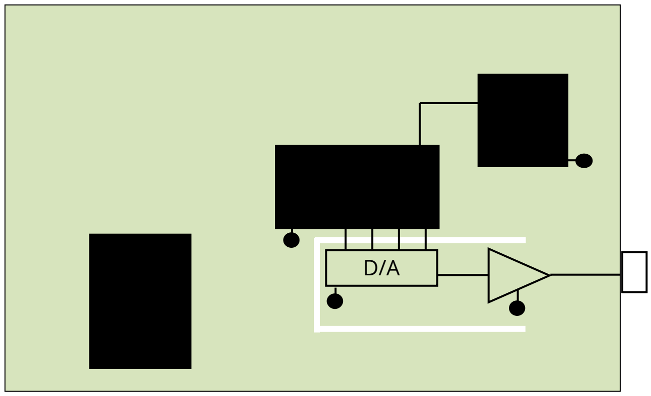
Ground vs. Signal Return

Exercise: Trace the path of the digital and analog return currents.



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Mixed-Signal Designs

If you have analog and digital returns that must be isolated (to prevent common-impedance coupling):

- Route the returns on separate conductors
- Provide a DC connection at the one point (or in the one area) where the reference potential must be the same.

Before isolating the returns, ALWAYS do this calculation to ensure that it is necessary!

$$\boxed{V_{max-coupled} = I_{max-source} \times R_{SHARED}}$$

Maximum shared resistance between the two circuits

Maximum voltage coupled to the victim circuit

Maximum current in the source circuit

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Mixed-Signal Designs

If you have analog and digital returns that must be isolated (to prevent common-impedance coupling):

- Route the returns on separate conductors
- Provide a DC connection at the one point (or in the one area) where the reference potential must be the same.
- This must include every place where a trace crosses the boundary between the analog and digital regions.

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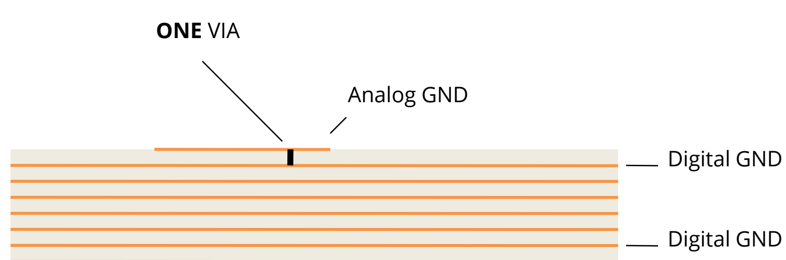
Sensitive A/D Isolation



If you think you need two vias, then you shouldn't be isolating the analog and digital grounds.

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Ground vs. Signal Return

You don’t need to gap a plane to control the flow of high frequency (>1MHz) currents. If you provide a low-inductance path for these currents to take, they will confine themselves to this path very well.

Rules for gapping a ground plane:

1. **Don’t do it!**
2. If you must do it, **never ever** allow a trace or another plane to cross over the gap.
3. If you must do it, **never ever** place a gap between two connectors.
4. Remember that the conductors on either side of the gap are at different potentials.
5. See Rule #1!

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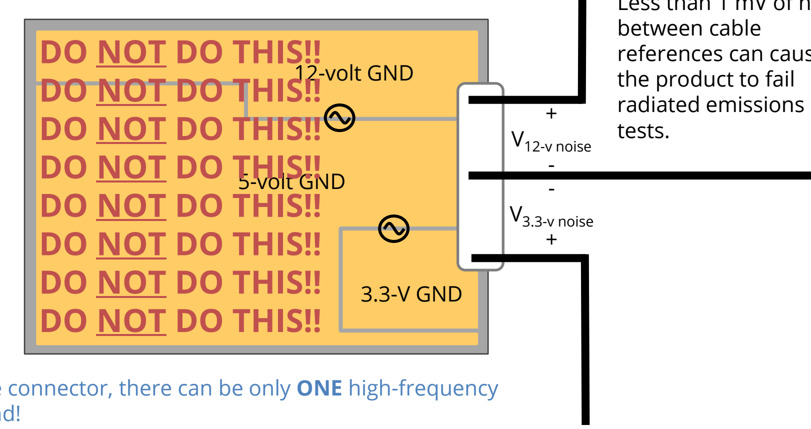
Provide 1 solid ground plane under all digital logic

Don’t Split Ground Planes!

Never let signals leave the board that are referenced to different high-frequency grounds.



Less than 1 mV of noise between cable references can cause the product to fail radiated emissions tests.

At the connector, there can be only **ONE** high-frequency ground!

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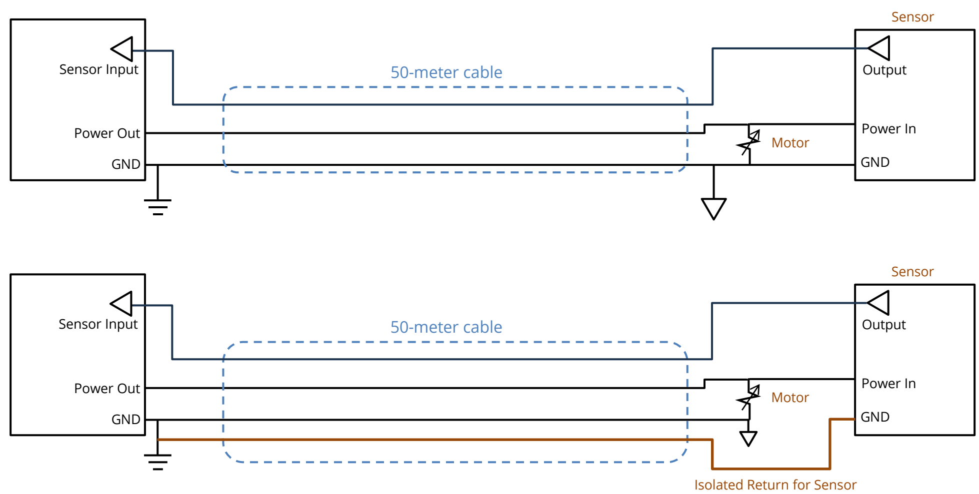
System-Level Low-Frequency Current-Return Example



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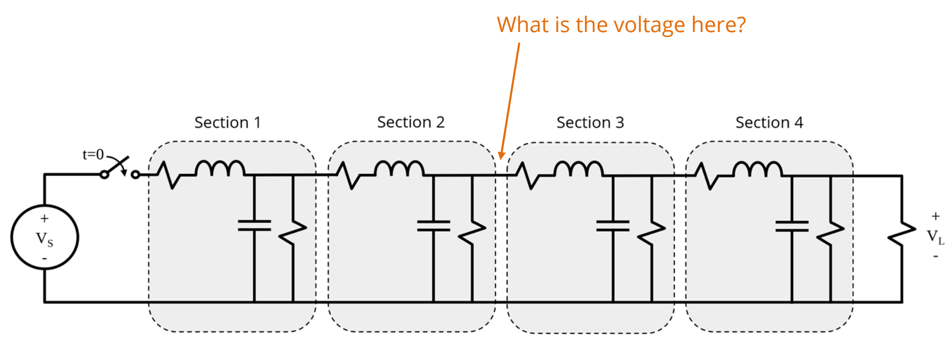
Ground in Circuit Simulations



The circuit simulation calculates a voltage, but it does not correspond to any real voltage in the system.

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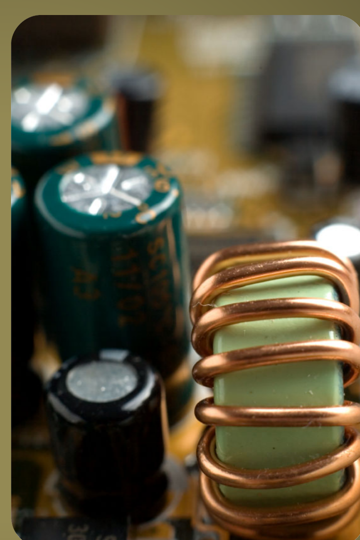
Key Points

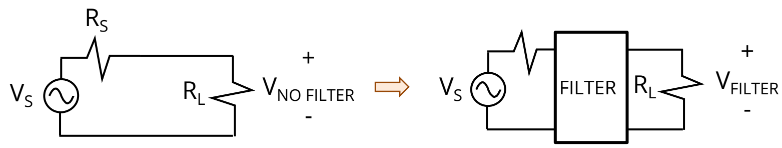
- Identify your HF ground and be sure it is the only ground that is large or connected to anything large!
- Don't call high-frequency current-carrying nets "ground". For example, refer to a current carrying analog reference net as "analog return".
- Be aware of where your HF and LF currents are flowing!
- Isolate returns only when necessary to control the flow of low frequency currents.
- **If you isolate two large conductors at low frequencies, be sure they are well connected at high frequencies.**

Filtering



General Definition of Insertion Loss

$$\text{Insertion Loss} = 10\log\frac{\text{Power Delivered to Load Without the Filter in Place}}{\text{Power Delivered to Load With the Filter in Place}}$$



$$IL = 10\log\left(\frac{\left(V_{NO\ FILTER}\right)^2}{R_L}\right) - 10\log\left(\frac{\left(V_{FILTER}\right)^2}{R_L}\right) = 20\log\left|\frac{V_{NO\ FILTER}}{V_{FILTER}}\right|$$

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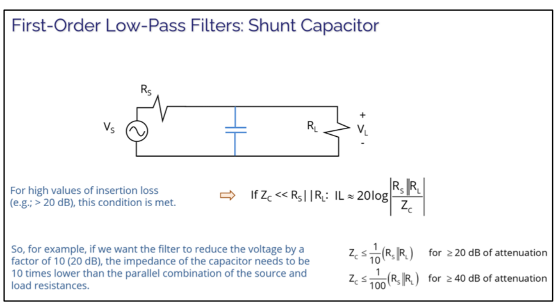
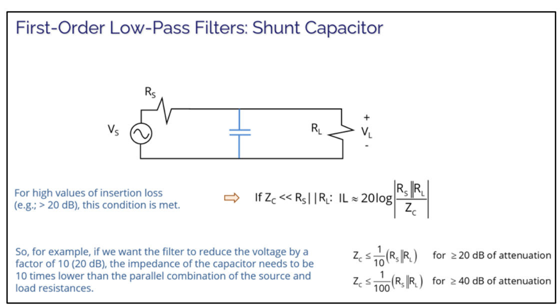
1st-Order Filters: Shunt Capacitors





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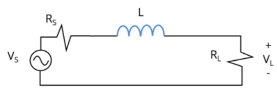
1st-Order Filters: Series Inductors

First-Order Low-Pass Filters: Series Inductor



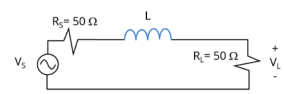
For high values of insertion loss (e.g.; > 20 dB), this condition is met. ⇨ If $Z_L >> R_S+R_L$: $IL \approx 20\log\left|\frac{R_S+R_L}{Z_L}\right|$

So, for example, if we want the filter to reduce the voltage by a factor of 10 (20 dB), the impedance of the inductor needs to be 10 times higher than the series combination of the source and load resistances.

$Z_L \geq 10(R_S+R_L)$ for ≥ 20 dB of attenuation
$Z_L \geq 100(R_S+R_L)$ for ≥ 40 dB of attenuation

Example

What value of series inductor is required to achieve at least 20 dB of attenuation at frequencies above 100 MHz?



$$\begin{aligned} Z_L &\geq 10(R_S+R_L) \quad \text{for } \geq 20 \text{ dB of attenuation} \\ &\geq 10(50+50) \\ &\geq 1000\ \Omega \end{aligned}$$

$$\omega L \geq 1000\ \Omega$$
$$L \geq \frac{1000\ \Omega}{2\pi \times 10^8}$$
$$L \geq 1.59 \times 10^{-6} \text{ henries} = 1.59\ \mu H$$

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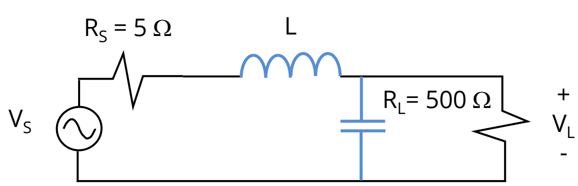
2nd–Order Filter for Low-Z Source and High-Z Load



- The inductor makes the source impedance look higher.
- The capacitor makes the load impedance look lower.

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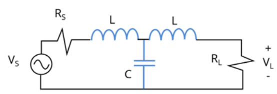
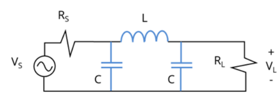
3rd-order Filters

T-Filter



- Provides attenuation for any combination of source and load resistances.
- Second-order filters like this exhibit greater attenuation at high frequencies.
- However, they may exhibit internal resonances or resonate with reactive loads.

Pi-Filter



- Every T-Filter has a Pi-Filter equivalent.
- Pi-Filters are generally preferred because inductors tend to be larger and more costly than capacitors in many applications. Less likely to resonate with capacitive loads.

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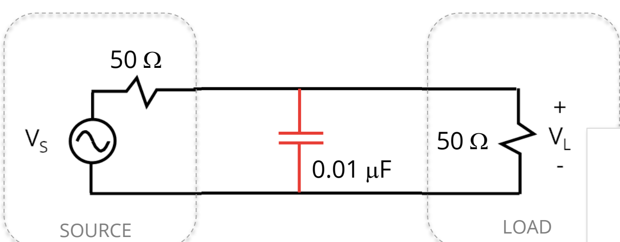
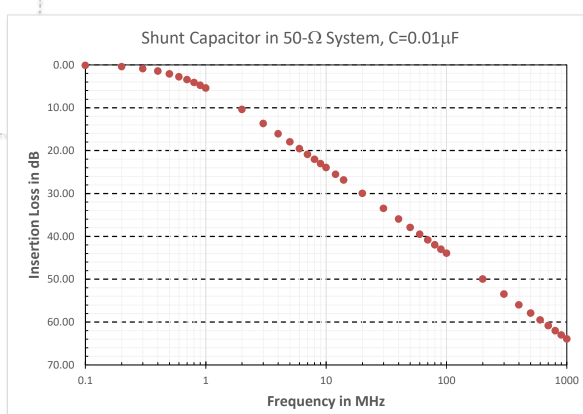
Simple Shunt Capacitor





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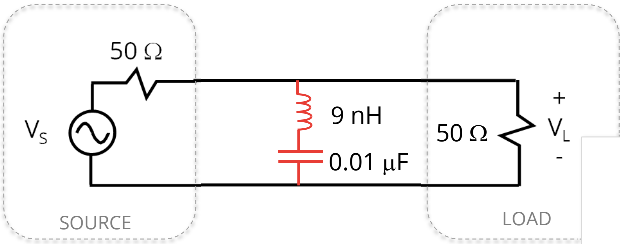
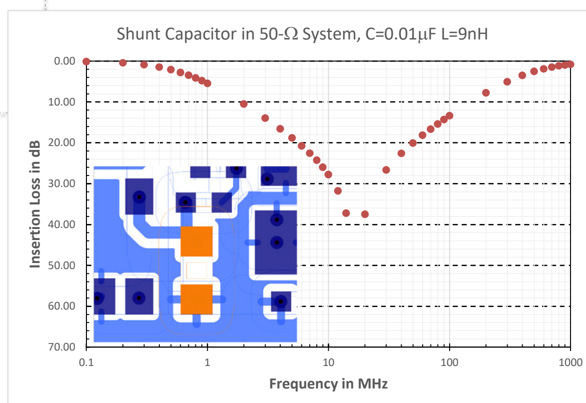
Simple Shunt Capacitor with Parasitic Inductance





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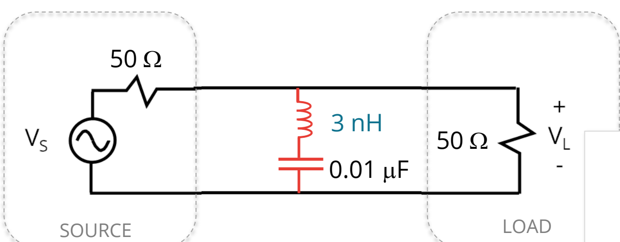
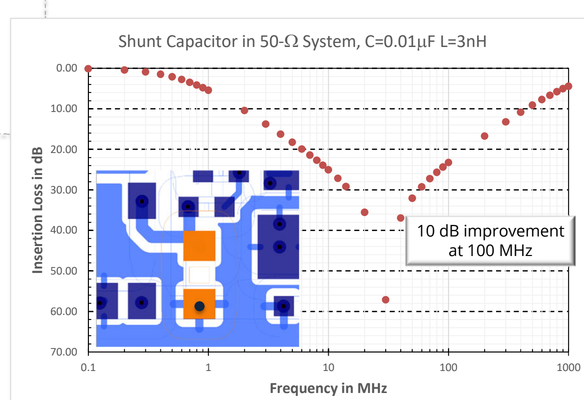
Simple Shunt Capacitor with Lower Parasitic Inductance





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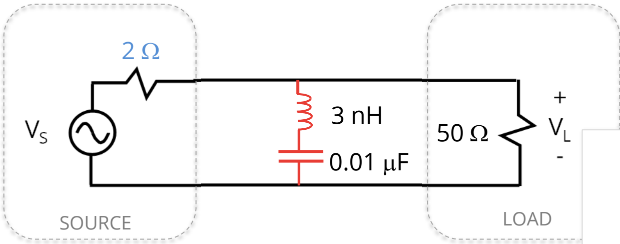
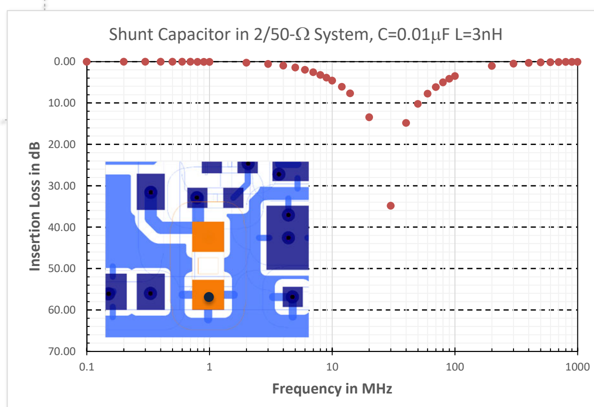
Simple Shunt Capacitor with Low-Impedance Source





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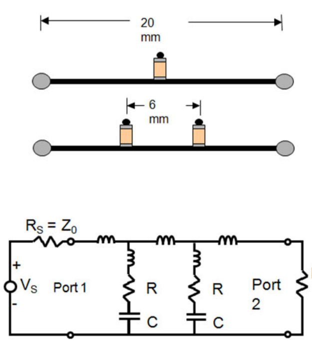
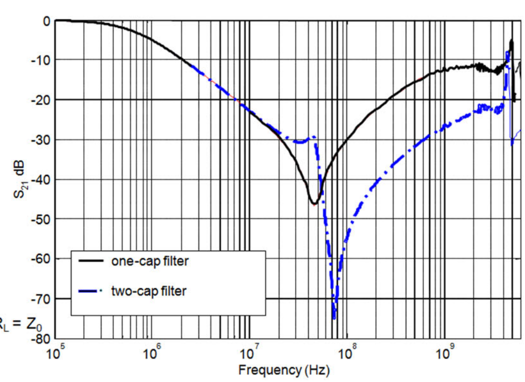
Filtering

Two capacitors can be more than twice as good as one.





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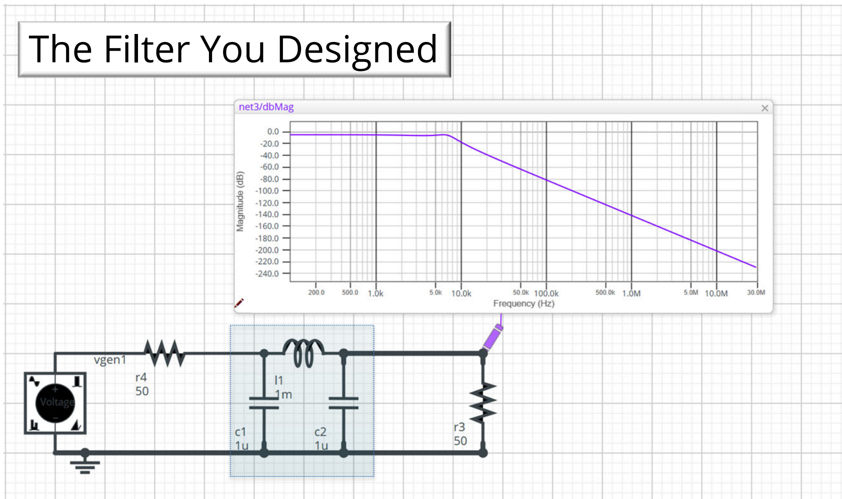
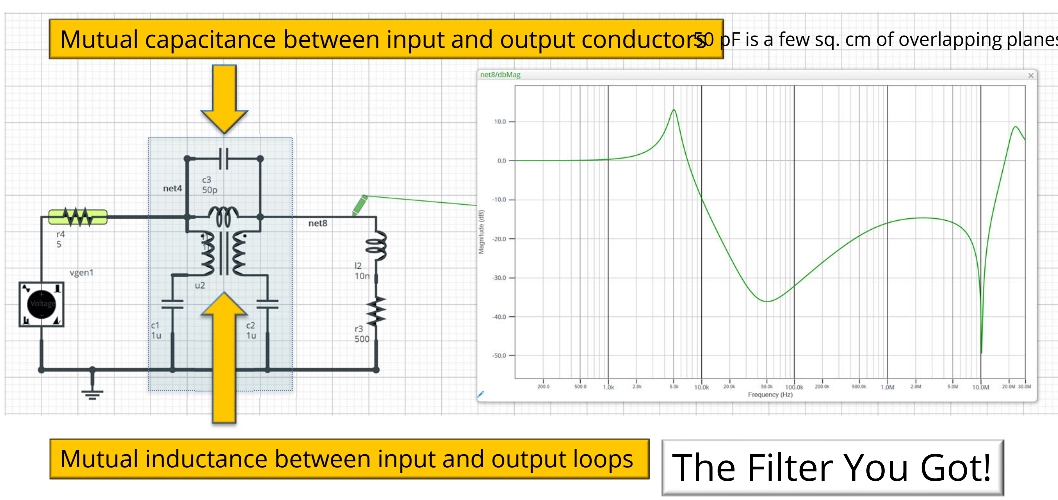
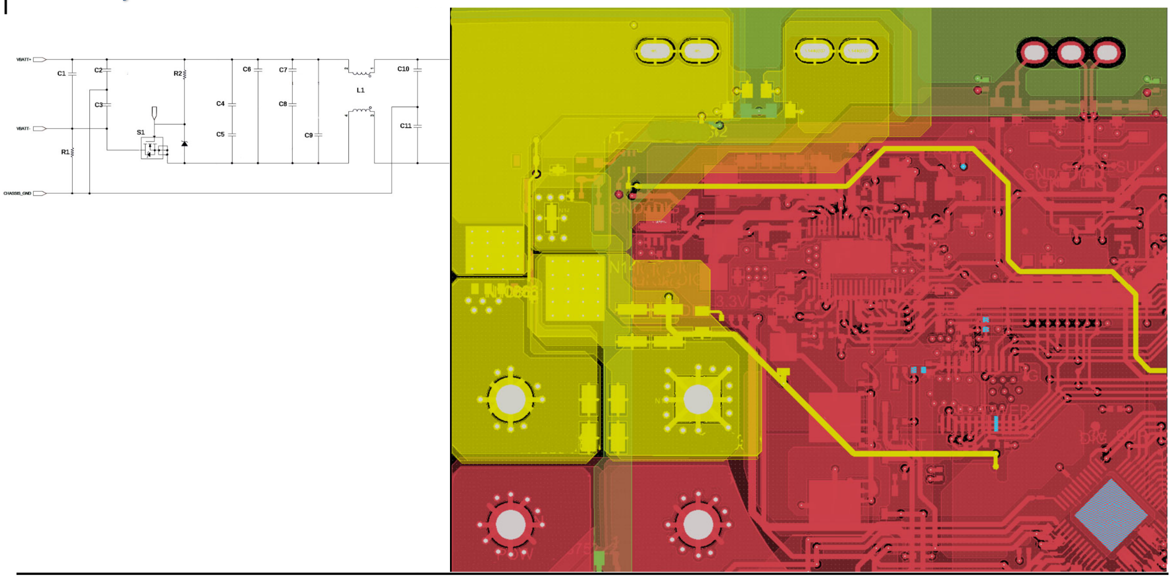
Effect of Component Parasitics



Effect of Component Parasitics



Identify the Nets on Both Sides of the Filter



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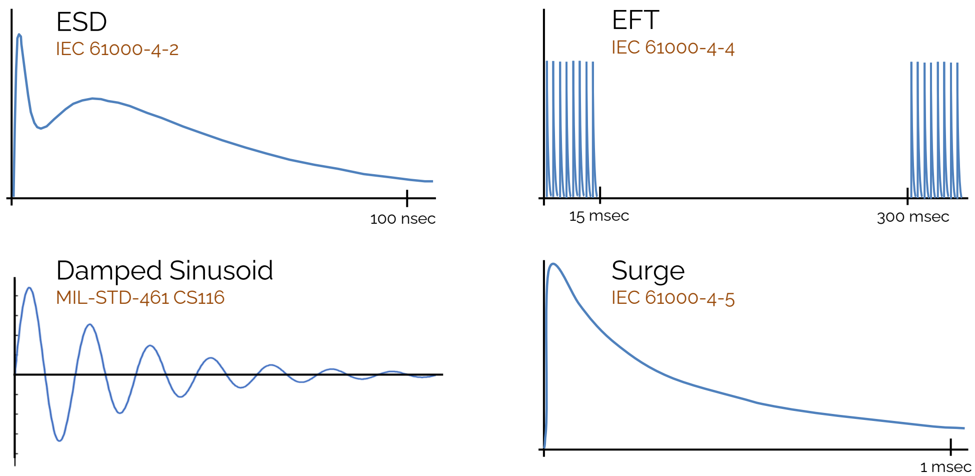
Electromagnetic Compatibility Principles and Design

Transient Protection

LearnEMC 2025 214

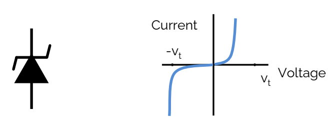
EMC Test Transients



Transient Protection Devices

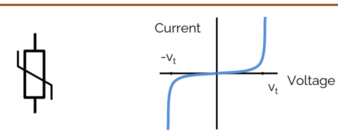
Diodes

0.5 volts to ~10 volts
Lowest Energy
High Capacitance
Usually fail short
Voltage limiting device



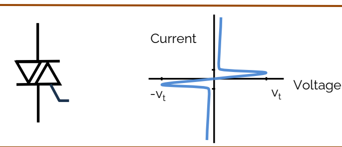
Varistors

0.5 volts to 10s of volts
Low Energy
High Capacitance
Usually fail short
Voltage limiting device



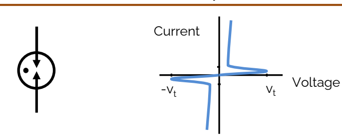
Thyristors

10s of volts to 100s of volts
Medium to High Energy
Moderate Capacitance
Usually fail open
Crowbar device



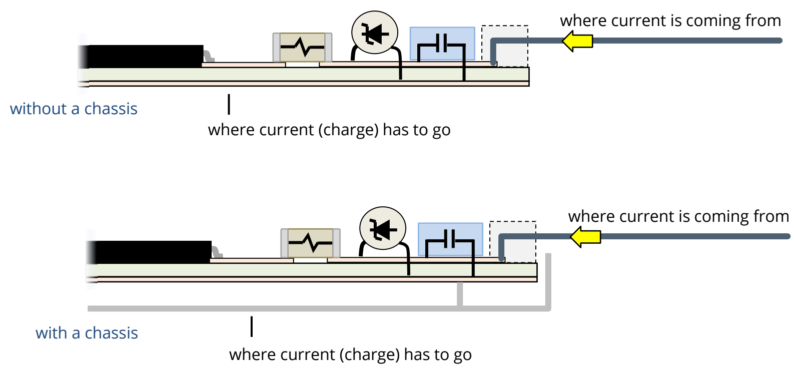
Gas Discharge Tubes

10s of volts to 1000s of volts
High Energy
Low Capacitance
Fail open
Crowbar device



Transient Protection

Help the transient current get to where it needs to go.



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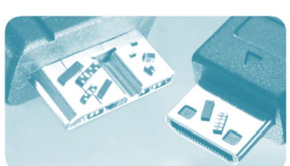
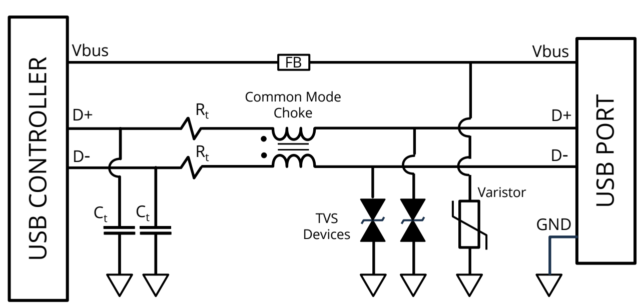
Options for High-Speed Interfaces





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Transient Protection ICs

NX20P0408
USB D+/D- protection IC
Rev. 1.1 — 19 August 2019 Product data sheet

1 General description

NX20P0408 is a single chip USB data lines protection solution that provides 28V short-to-VBUS protection to system side D+ and D- pins located near VBUS pins.

USB Type-C allows VBUS voltage to increase up to 20V through Power delivery protocol. D+ and D- pins can be shorted to VBUS due to mechanical twisting and sliding of the connector since Type-C connector contact pins are 25% closer to each other than a micro USB connector. Moisture or fine dust may also cause the 20V VBUS pin to be shorted to adjacent pins.

NX20P0408 enables D+/D- to be robust in even abnormal conditions. NX20P0408 is 28V DC tolerant on D+/D- pin in connector side and quickly disconnects switches if the voltage is above overvoltage threshold, protecting D+/D- in system side from high voltage.

2 Features and benefits

- USB Type-C D+/D- short protection to VBUS
  - CON_DP / CON_DN : $28V_{DC}$
- Low Rdson switch : 4Ω
- High switch bandwidth = 1.5GHz
- 35V surge protection on CON_DP/CON_DN
- Fast OVP turn off time : 60ns
- Post-stage clamp circuit to clamp voltage until switch is off.

3 Applications

- Smartphone
- Tablet
- Laptop

5 Functional diagram

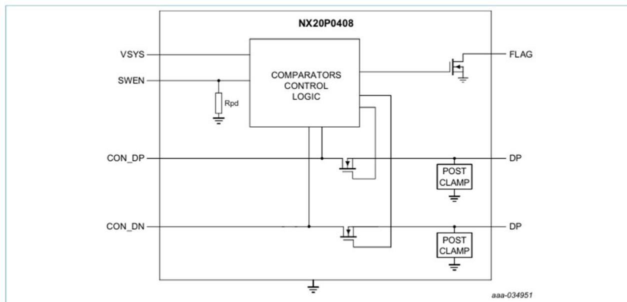
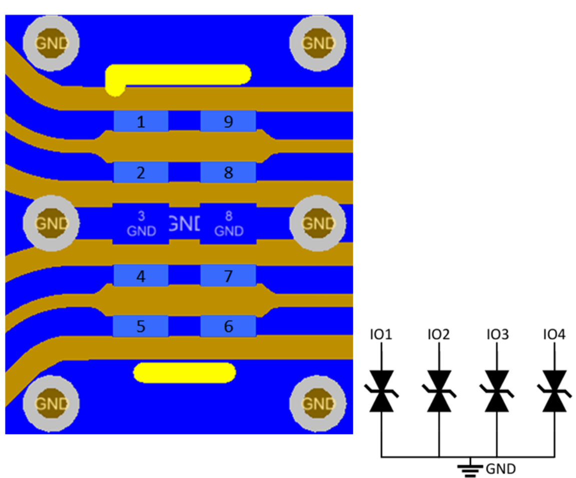


Figure 1. Block diagram

USB and HDMI Transient Protection



Product Folder | Sample & Buy | Technical Documents | Tools & Software | Support & Community

Texas Instruments

TPD4E02B04
SLVSD85B – NOVEMBER 2015 – REVISED JULY 2016

TPD4E02B04 4-Channel ESD Protection Diode for USB Type-C and HDMI 2.0

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±12-kV Contact Discharge
  - ±15-kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 2 A (8/20 µs)
- IO Capacitance:
  - 0.25 pF (Typical)
  - 0.33 pF (Maximum)
- DC Breakdown Voltage: 5.5 V (Minimum)
- Ultra Low Leakage Current: 10 nA (Maximum)
- Low ESD Clamping Voltage: 8.8 V at 5-A TLP
- Supports High Speed Interfaces up to 10 Gbps
- Industrial Temperature Range: –40°C to +125°C
- Easy Flow-Through Routing Package
- Interfaces
  - USB Type-C
  - USB 3.1 Gen 2
  - HDMI 2.0/1.4
  - USB 3.0
  - DisplayPort 1.3
  - PCI Express 3.0

2 Applications

- End Equipment
  - Laptops and Desktops
  - Set-Top Boxes
  - TV and Monitors
  - Mobile and Tablets
  - DVR and NVR

3 Description

The TPD4E02B04 is a bidirectional TVS ESD protection diode array for USB Type-C and HDMI 2.0 circuit protection. The TPD4E02B04 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

This device features a 0.25-pF IO capacitance per channel making it ideal for protecting high-speed interfaces up to 10 Gbps such as USB 3.1 Gen2. The low dynamic resistance and low clamping voltage ensure system level protection against transient events.

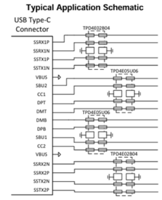
The TPD4E02B04 is offered in the industry standard USON-10 (DQA) package. The package features flow-through routing and 0.5-mm pin pitch easing implementation and reducing design time.

Device Information(1)

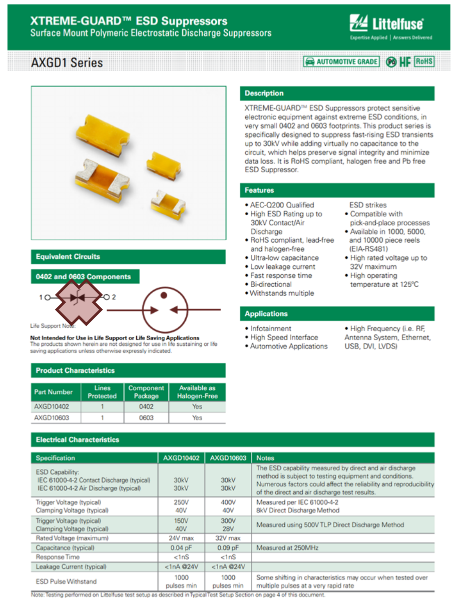
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4E02B04	USON (10)	2.50 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Low-Capacitance ESD Protection



XTREME-GUARD™ ESD Suppressors
Surface Mount Polymeric Electrostatic Discharge Suppressors

Littelfuse
Expertise Applied | Answers Delivered

AXGD1 Series

AUTOMOTIVE GRADE HF RoHS

Description

XTREME-GUARD™ ESD Suppressors protect sensitive electronic equipment against extreme ESD conditions, in very small 0402 and 0603 footprints. This product series is specifically designed to suppress fast-rising ESD transients up to 30kV while adding virtually no capacitance to the circuit, which helps preserve signal integrity and minimize data loss. It is RoHS compliant, halogen free and Pb free ESD Suppressor.

Features

- AEC-Q200 Qualified
- High ESD Rating up to 30kV Contact/Air Discharge
- RoHS compliant, lead-free and halogen-free
- Ultra-low capacitance
- Low leakage current
- Fast response time
- Bi-directional
- Withstands multiple ESD strikes
- Compatible with pick-and-place processes
- Available in 1000, 5000, and 10000 piece reels (EIA-RS481)
- High rated voltage up to 32V maximum
- High operating temperature at 125°C

Equivalent Circuits

0402 and 0603 Components

1 2

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications
The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Applications

- Infotainment
- High Speed Interface
- Automotive Applications
- High Frequency (i.e. RF, Antenna System, Ethernet, USB, DVI, LVDS)

Product Characteristics

Part Number	Lines Protected	Component Package	Available as Halogen-Free
AXGD10402	1	0402	Yes
AXGD10603	1	0603	Yes

Electrical Characteristics

Specification	AXGD10402	AXGD10603	Notes
ESD Capability: IEC 61000-4-2 Contact Discharge (typical) IEC 61000-4-2 Air Discharge (typical)	30kV 30kV	30kV 30kV	The ESD capability measured by direct and air discharge method is subject to testing equipment and conditions. Numerous factors could affect the reliability and reproducibility of the direct and air discharge test results.
Trigger Voltage (typical) Clamping Voltage (typical)	250V 40V	400V 40V	Measured per IEC 61000-4-2 8kV Direct Discharge Method
Trigger Voltage (typical) Clamping Voltage (typical)	150V 40V	300V 28V	Measured using 500V TLP Direct Discharge Method
Rated Voltage (maximum)	24V max	32V max	
Capacitance (typical)	0.04 pF	0.09 pF	Measured at 250MHz
Response Time	<1nS	<1nS	
Leakage Current (typical)	<1nA @24V	<1nA @24V	
ESD Pulse Withstand	1000 pulses min	1000 pulses min	Some shifting in characteristics may occur when tested over multiple pulses at a very rapid rate

Note: Testing performed on Littelfuse test setup as described in Typical Test Setup Section on page 4 of this document.

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Electromagnetic Compatibility Principles and Design

Shielding

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Coupling Paths

Shielding strategies depend on the type of coupling.

- Conducted Coupling ← Don't use shielding.
- Electric Field Coupling ← Use a good conductor (e.g., metal) appropriately grounded.
- Magnetic Field Coupling ← < 1kHz use magnetic materials. > 10 kHz use good conductors.
- Radiation Coupling ← Use E-Field and/or H-Field shielding to prevent coupling to the unintentional transmitting or receiving antenna

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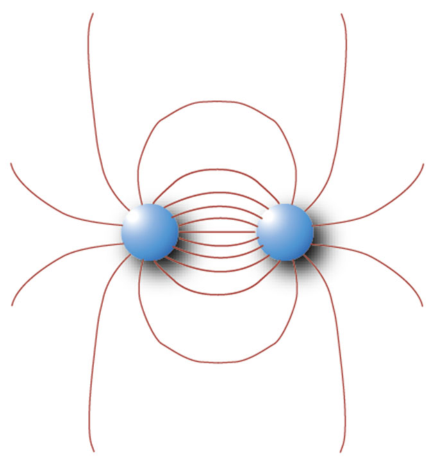
Charge, Voltage and Electric Fields



- Electric field lines start on positive charge and end on negative charge.
- Electric field lines start on conductors with one voltage and terminate on conductors with a lower voltage.

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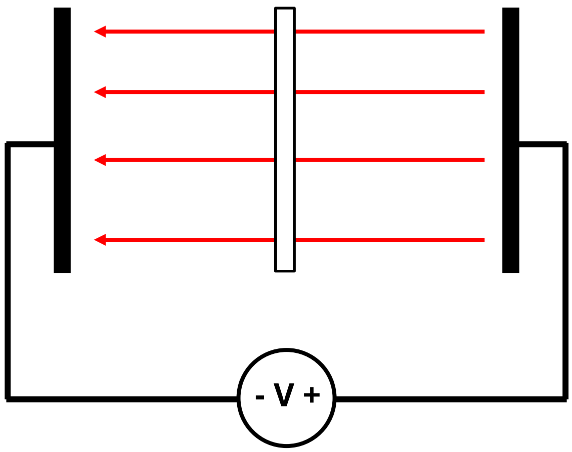
Electric Field Shielding



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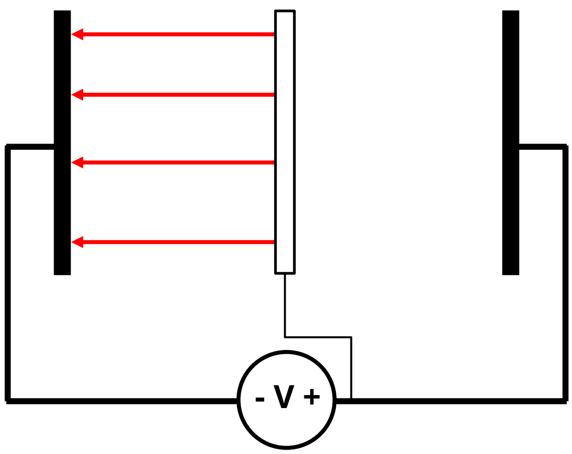
Electric Field Shielding



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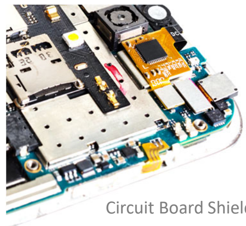
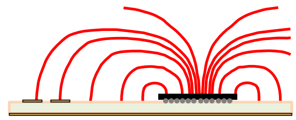
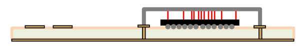
Electric-Field Shielding Examples

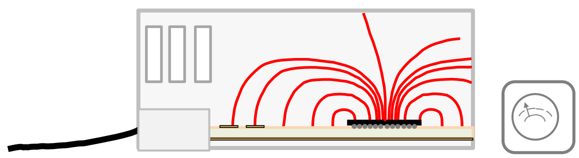


Circuit Board Shields





Enclosure Shield



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Summary of Electric Field Shielding

- Any two conductors at different potentials (voltages) have electric field lines between them.
- It is important to be able to visualize the electric field in order to mitigate coupling effectively.
- Shielding involves capturing and redirecting the electric field.
- Materials to use: Good conductors such as copper, aluminum, steel, etc.
- Electric field shields are usually connected to something labeled “ground”.

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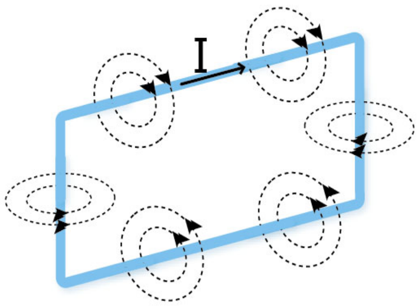
Magnets, Current and Magnetic Fields



- Magnetic field lines circulate around flowing electric charge (current).
- Lines of magnetic field do not start or stop. They always close on themselves.

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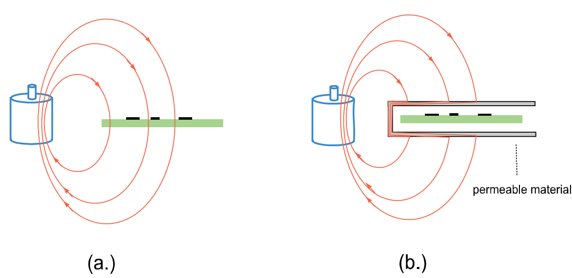
Low-Frequency Magnetic-Field Shielding

Magnetic Field Shielding

(at low frequencies)



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LF Magnetic Shielding Materials

Material	Relative Permeability
Gold, copper, aluminum	1
Concrete, water, air, vacuum	1
Ferrite U60 (UHF Chokes)	8
Common Steel	
Pure Nickel	600
Ferrite M33 (inductors)	750
Pure Iron	5,000
Permalloy (20% iron, 80% nickel)	8,000
Ferrite T38 (RF Transformers)	10,000
Mu-metal	20,000 – 50,000
Supermalloy (recording heads)	100,000

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Summary of LF Magnetic Field Shielding

- You can't stop a magnetic flux line; you can only redirect it.
- It is important to be able to visualize the magnetic field to mitigate coupling effectively.
- Shielding involves capturing and redirecting the magnetic field.
- Materials to use: high permeability materials such as steel or iron-nickel alloys.
- Grounding does not affect the shielding effectiveness of LF magnetic field shields.

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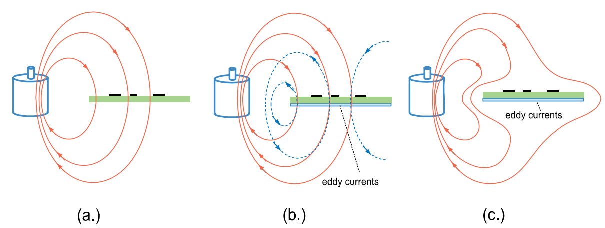
High-Frequency Magnetic-Field Shielding

Magnetic Field Shielding

(at high frequencies)



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Summary of HF Magnetic Field Shielding

- You can't stop a magnetic flux line; you can only redirect it.
- At frequencies above a few kHz, magnetic flux lines will not pass through good conductors due to eddy currents induced in these conductors.
- Shielding involves redirecting the magnetic field.
- Materials to use: thick aluminum, copper or steel plates.
- Grounding does not affect the shielding effectiveness of HF magnetic field shields.

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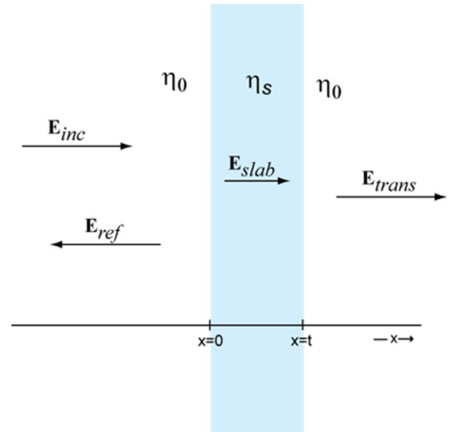
Plane Wave Shielding Theory

$$\left|\mathbf{E}_{trans}\right| = \left|\mathbf{E}_{inc}\right| \frac{2\eta_s}{\eta_0+\eta_s}\left(\frac{2\eta_0}{\eta_0+\eta_s}\right)e^{-t/\delta}$$



For good conductors:

$$\eta = \sqrt{\frac{j\omega\mu}{\sigma+j\omega\varepsilon}} \approx \sqrt{\frac{j\omega\mu}{\sigma}} = \sqrt{\frac{\omega\mu}{\sigma}}e^{j\pi/4}$$

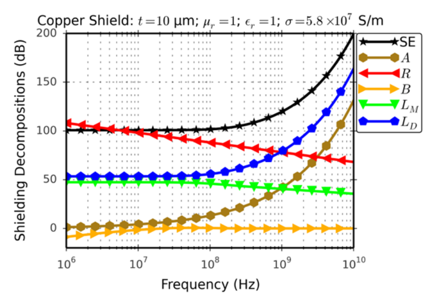
$$S.E. = 20\log\frac{E_{inc}}{E_{trans}}$$

$$S.E. = 20\log\frac{\eta_0}{4\eta_s} \quad + \quad 20\log e^{t/\delta} = R(dB) \quad + \quad A(dB)$$

Note: These are NOT accurate representations of the relative amounts of power reflected and absorbed.

Plane Wave Shielding Theory

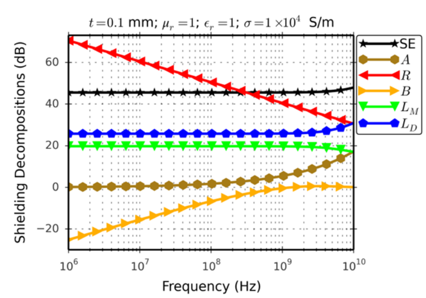
Copper
(10 μm thick)



Schelkunoff decomposition:
SE (dB) = R(dB) + A(dB) + B(dB)

Mismatch decomposition:
SE (dB) = L_M(dB) + L_D(dB)

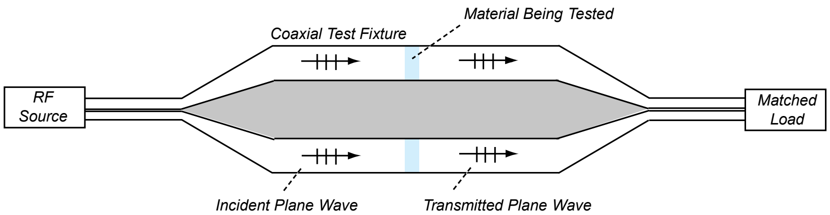
Nanofiber Composite
(100 μm thick)



A. McDowell and T. Hubing, "Analysis and comparison of plane wave shielding effectiveness decompositions," IEEE Trans. on Electromagnetic Compatibility, vol. 56, no. 6, Dec. 2014, pp. 1711-1714.

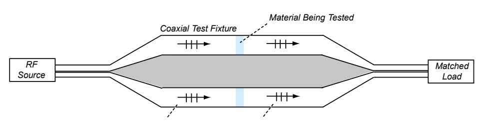
Plane Wave Shielding Effectiveness

Shielding Effectiveness Measurements



$$\text{S.E.} = 10\log\frac{\text{power received at the termination}}{\text{forward power from the source}}$$

Quiz



A shield made of a material with a shielding effectiveness of **100 dB** will reduce the radiation from an enclosed source by,

a.) 100 dB

b.) at least 100 dB

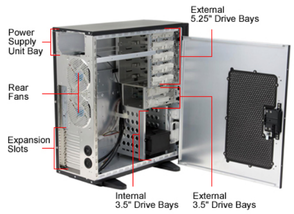
c.) between 0 dB and 100 dB

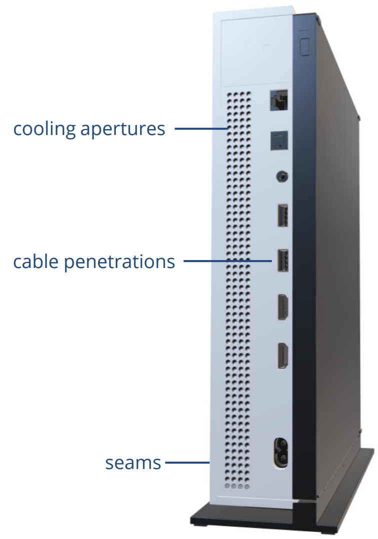
d.) possibly less than 0 dB

Real shields are ALWAYS in the near field of either the source or victim!

They need to be modeled as part of the radiating structure (antenna).

Enclosure Shielding





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Gauss' Law and the Faraday Cage

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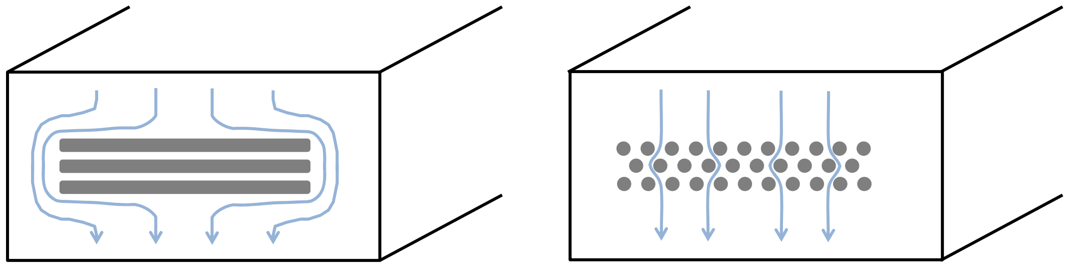
Apertures

Small apertures that allow current to flow unimpeded do not reduce the enclosure shielding effectiveness significantly.



Many small, round apertures are preferable to thin slots with the same cooling area.

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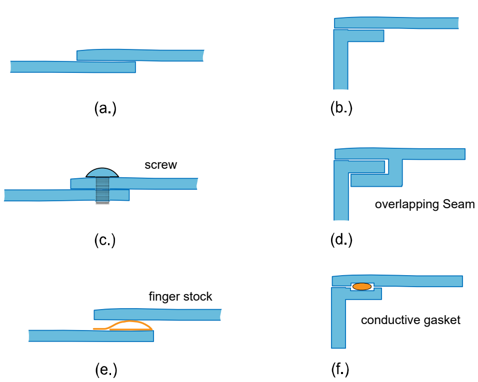
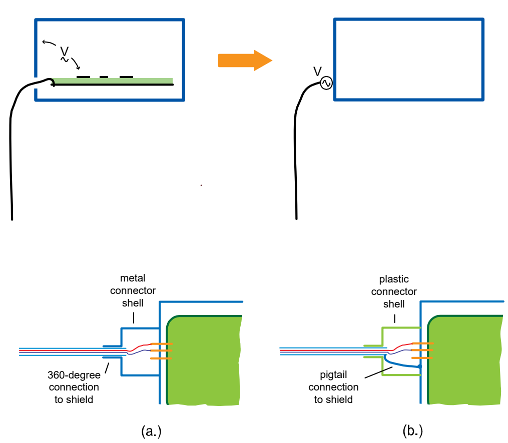
Shielding Enclosures



Treatment of Seams



Treatment of Wire Penetrations

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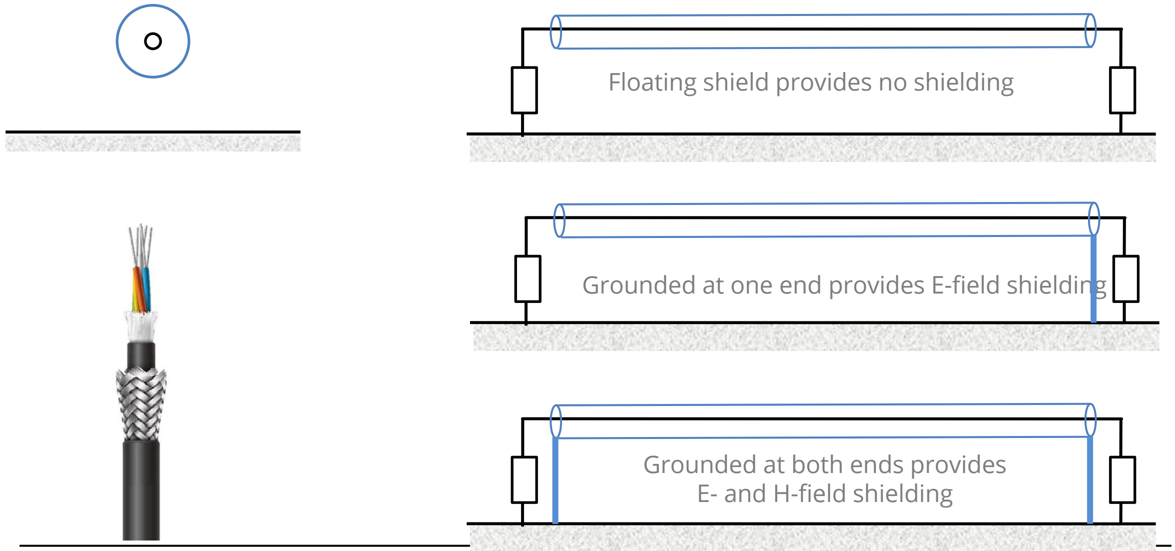
Cable Shields (short relative to λ/4)



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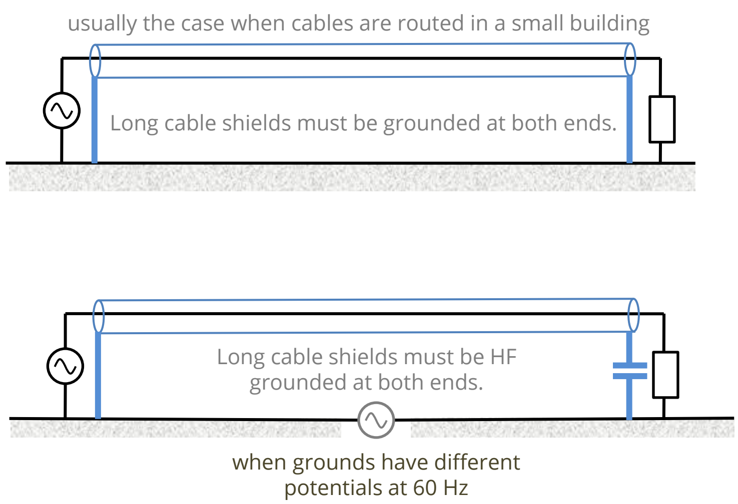
Cable Shields (long relative to λ)



Ten amperes of current flowing in a cable shield is not inherently unsafe. However, if the shield connection is broken, an L di/dt voltage appears at the open connection and the energy stored in the loop inductance can be discharged at that point.

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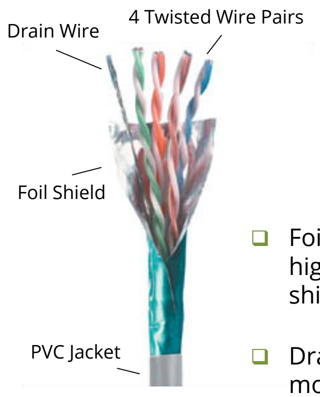
Anatomy of a Cable Shield



CAT5e Cable

- Foil provides high-frequency shielding.
- Drain wire carries most of the low-frequency current.

- Foil provides high-frequency shielding.
- Braid carries strong current at lower frequencies.

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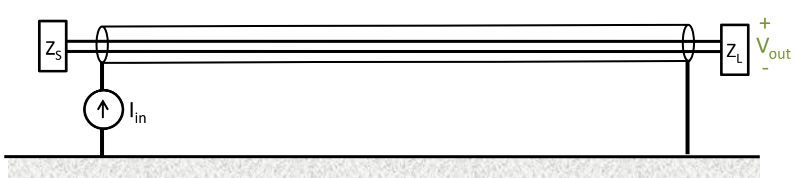
Transfer Impedance Measurements

$$Z_{transfer} = V_{out} / I_{in}$$



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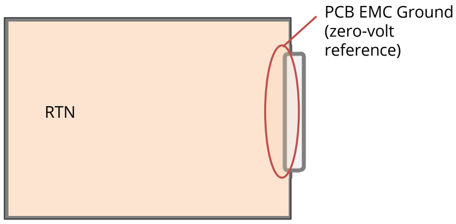
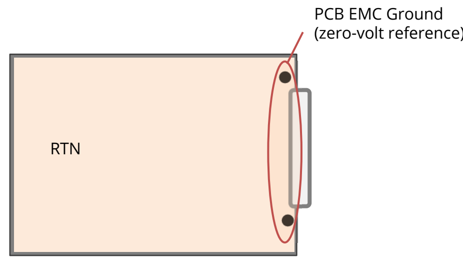
Connecting Cable Shields on the PCB

- Cable shields should ALWAYS connect directly to the chassis.
- If they must connect to the board first, it must be to the PCB EMC Ground.
- If the cable shield returns intentional current, it must ALSO connect to the circuit board return plane.



PCB in product with no ground structure



PCB mounted near the ground structure

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Summary of Cable Shielding

- Serves different purposes in different applications.
- Sometimes carries intentional signal currents. Shield terminations become critical.
- May prevent coupling of external electric or magnetic fields to signals carried by wires in the cable.
- Beware of transfer impedance data. It should only be used to compare similar cables for a similar application measured with the same test set-up.

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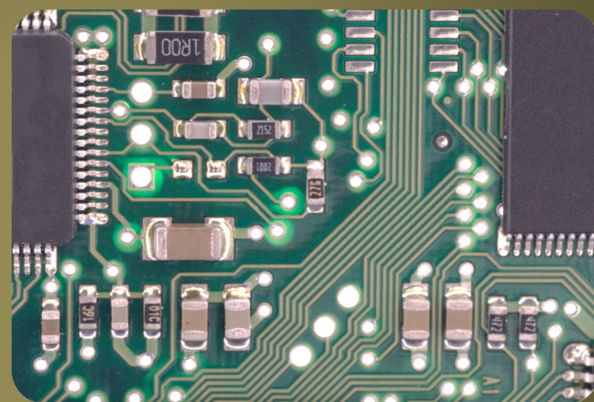
Electromagnetic Compatibility Principles and Design

DC Power Distribution and Decoupling



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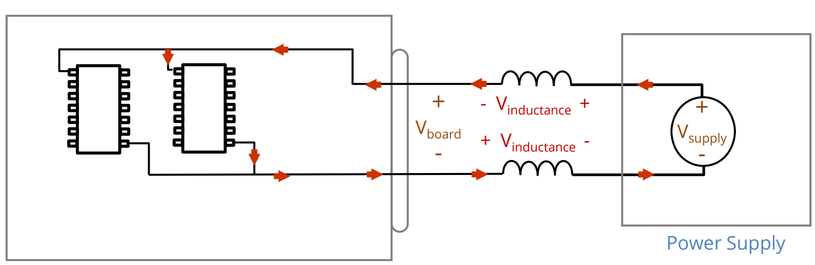
The Concept of Power Bus Decoupling



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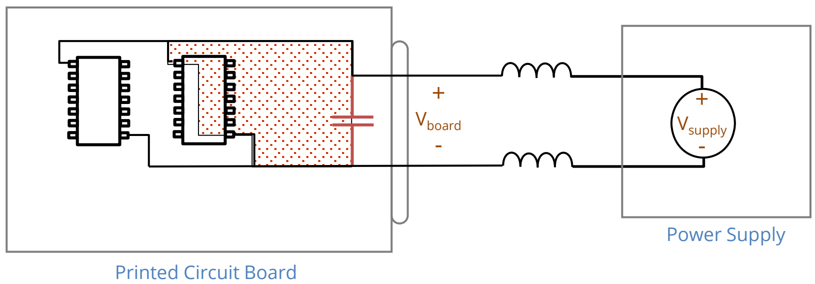
The Concept of Power Bus Decoupling



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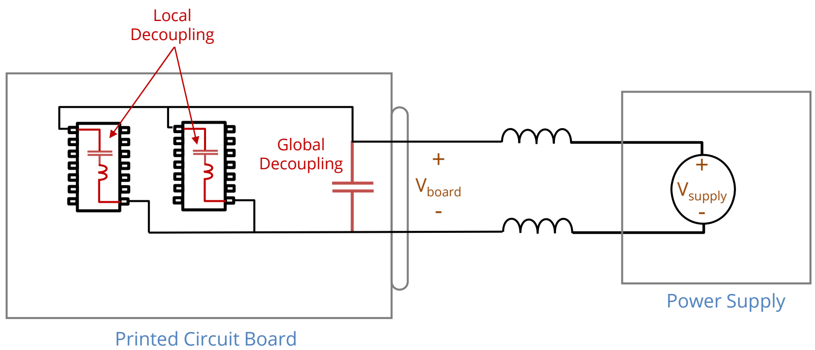
The Concept of Power Bus Decoupling



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Rules for PCB Decoupling?

Use small-valued capacitors for high-frequency decoupling.

Locate capacitors near the power pins of active devices.

Use 0.1 μF for local decoupling!

Use capacitors with a low ESR!

Avoid capacitors with a low ESR!

Use 0.01 μF for local decoupling!

Run traces from device to capacitor, then to power planes.

Locate capacitors near the ground pins of active devices.

Location of decoupling capacitors is not relevant.

Never put traces on decoupling capacitors.

Local decoupling capacitors should have a range of values from 100 pF to 1 μF!

Use the largest valued capacitors you can find in the smallest package size.

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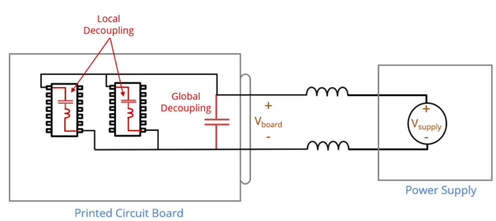
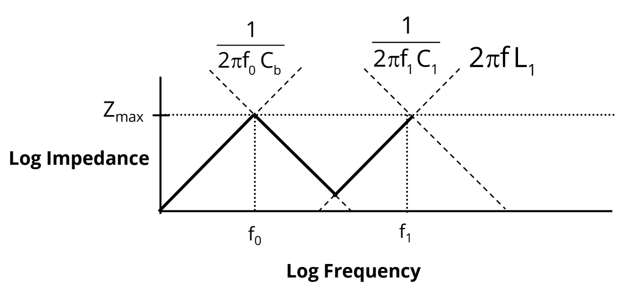
How much capacitance do you need?

Impedance Approach

$$Z_{max} = \frac{V_{noise\_max}(f)}{I_{device\_max}(f)}$$





$$\frac{1}{2\pi f C} \leq Z_{max}$$

$$C \geq \frac{1}{2\pi f Z_{max}}$$

$$\geq \frac{1}{(2\pi f_0)^2 L_{source}}$$

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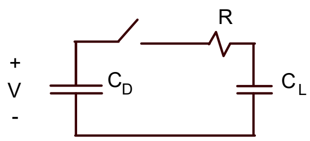
How much capacitance do you need?

Capacitance Ratio Approach

Recognizing that CMOS loads are capacitances, we are simply using decoupling capacitors to charge load capacitances.



Total decoupling capacitance is set to a value that is equal to the total device capacitance times the power bus voltage divided by the maximum power bus noise.

Guidelines Approach

Let's do it the way that worked for somebody at sometime in the past.

For Example: Include one 0.01 μF local decoupling capacitor for each VCC pin of every active component on the board plus 1 bulk decoupling capacitor with a value equal to 5 times the sum of the local decoupling capacitance." .

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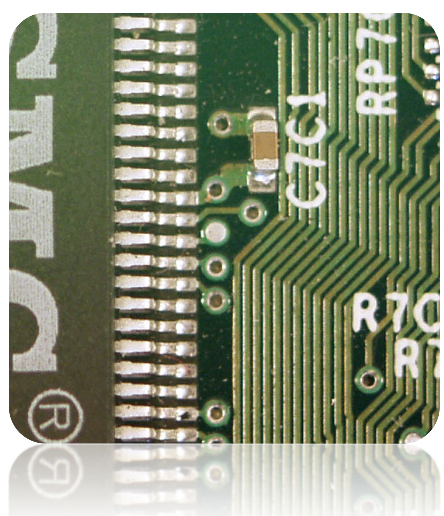
Printed Circuit Board Decoupling Layout



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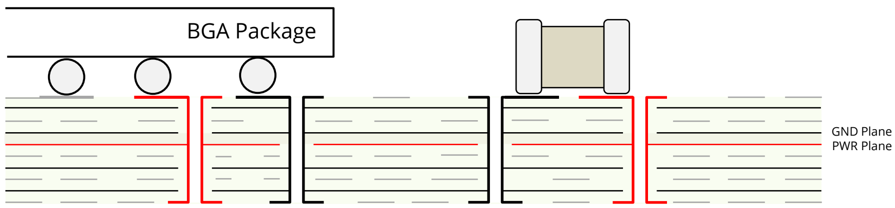
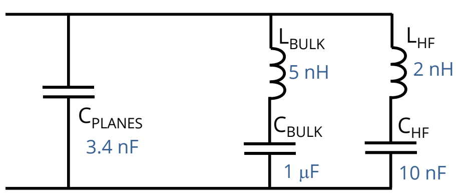
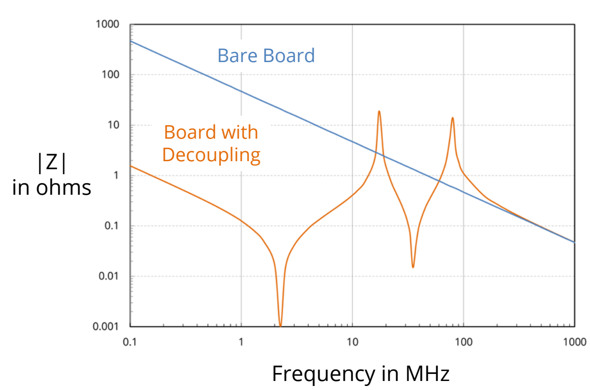
Boards with Closely Spaced Power Planes



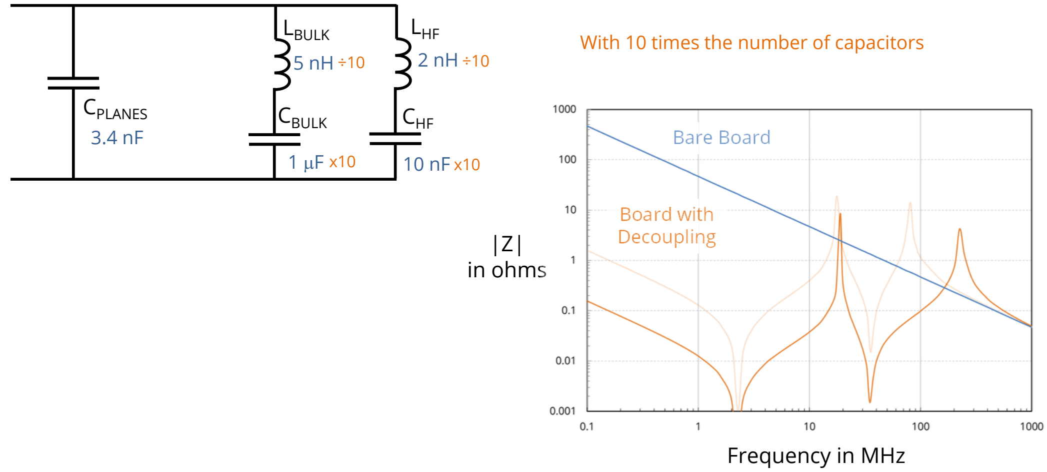
Power Distribution Model ~ (5 - 500 MHz)
(Board with power and power return planes less than 0.5 mm apart)

Boards with Closely Spaced Power Planes





Boards with Closely Spaced Power Planes



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For Boards with "Closely-Spaced" Planes

- The location of the decoupling capacitors is not critical.
- The value of the high-frequency decoupling capacitors is not critical, but it must be greater than the interplane capacitance.
- The inductance of the connection is the most important parameter of a high-frequency decoupling capacitor.
- None of the high-frequency decoupling capacitors are effective above a couple hundred megahertz.
- None of the high-frequency decoupling capacitors are supplying significant charge in the first few nanoseconds of a transition.

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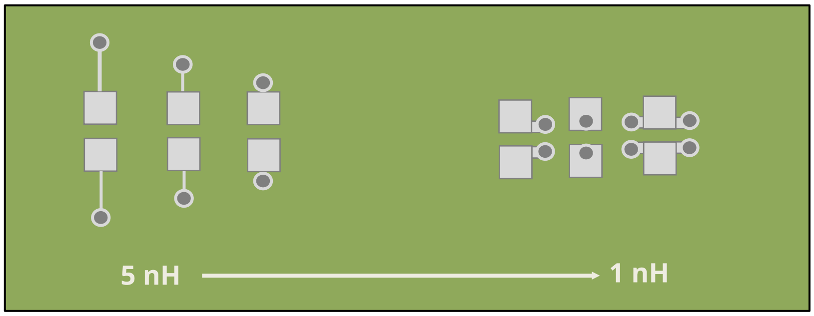
Inductance of Connections to Planes

0402 capacitors mounted one or two layers above closely spaced power and ground planes



Generally, 100 decoupling capacitors connected through 1 nH of inductance will be as effective as 500 decoupling capacitors connected through 5 nH of inductance.

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Power Bus Decoupling Strategy

With closely spaced (<.25 mm) planes

- all decoupling capacitors are global
- size global decoupling to meet board requirements
- mount local decoupling in most convenient locations
- don't put traces on capacitor pads
- too much capacitance is ok
- too much inductance is not ok

References:

T. H. Hubing, J. L. Drewniak, T. P. Van Doren, and D. Hockanson, "Power Bus Decoupling on Multilayer Printed Circuit Boards," *IEEE Transactions on Electromagnetic Compatibility*, vol. EMC-37, no. 2, May 1995, pp. 155-166.

T. Zeeff and T. Hubing, "Reducing power bus impedance at resonance with lossy components," IEEE Transactions on Advanced Packaging, vol. 25, no. 2, May 2002, pp. 307-310.

M. Xu, T. Hubing, J. Chen, T. Van Doren, J. Drewniak and R. DuBroff, "Power bus decoupling with embedded capacitance in printed circuit board design," IEEE Transactions on Electromagnetic Compatibility, vol. 45, no. 1, Feb. 2003, pp. 22-30.

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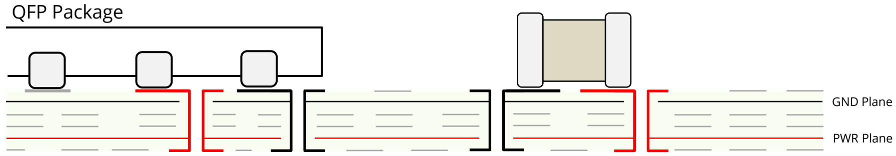
Boards with Widely Spaced Power Planes



Power Distribution Model ~ (5 - 500 MHz)
(Board with power and power return planes greater than 0.75 mm apart)

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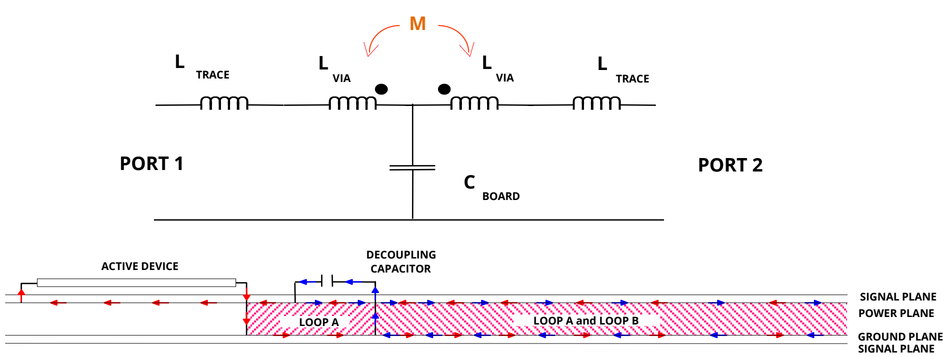
Boards with Power Planes Spaced >0.5 mm



On boards with a spacing between power and ground planes of ~30 mils (0.75 mm) or more, the inductance of the planes can no longer be neglected. In particular, the mutual inductance between the vias of the active device and the vias of the decoupling capacitor is important. The mutual inductance will tend to cause the majority of the current to be drawn from the nearest decoupling capacitor and not from the planes.

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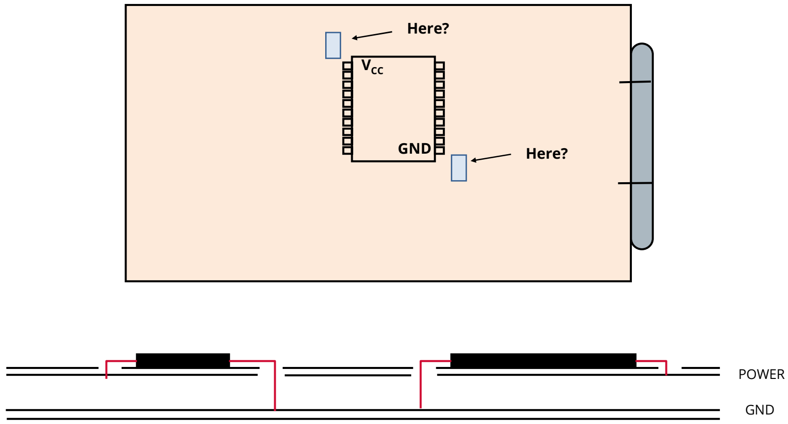
Where do I mount the capacitor?



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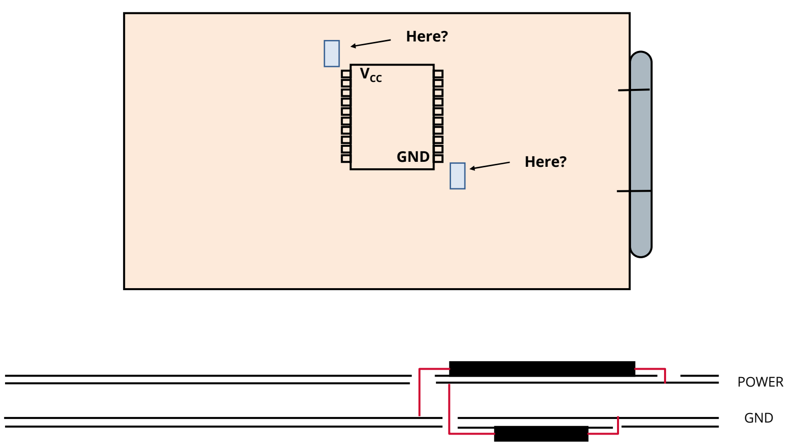
Where do I mount the capacitor?



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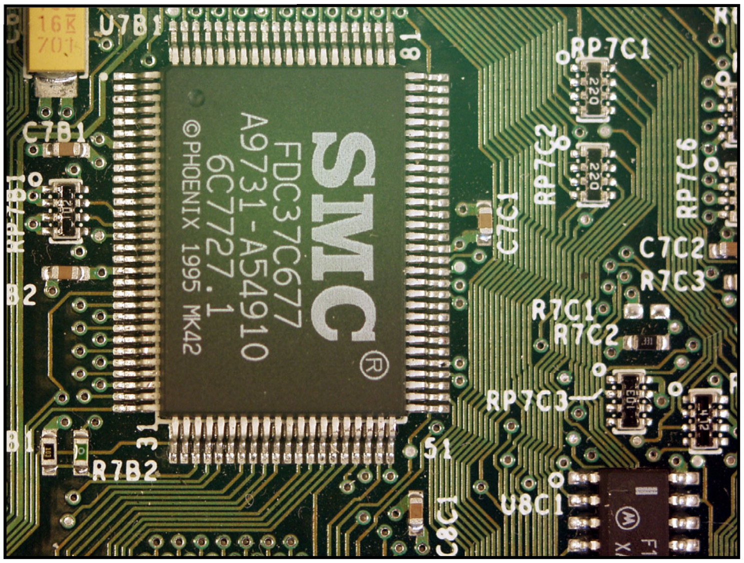
6-Layer Board Decoupling



For Boards with "Widely-Spaced" Planes

- Local decoupling capacitors should be located as close to the active device as possible (near pin attached to most distant plane).
- The value of the local decoupling capacitors should be 10,000 pF or greater.
- The inductance of the connection is the most important parameter of a local decoupling capacitor.
- Local decoupling capacitors can be effective up to 1 GHz or higher if they are connected properly.

Power Bus Decoupling Strategy

With widely spaced (>.5 mm) planes

- size bulk decoupling to meet board requirements
- size local decoupling to meet device requirements
- mount local decoupling near pin connected to furthest plane
- don't put traces on capacitor pads
- too much capacitance is ok
- too much inductance is not ok

References:

J. Chen, M. Xu, T. Hubing, J. Drewniak, T. Van Doren, and R. DuBroff, "Experimental evaluation of power bus decoupling on a 4-layer printed circuit board," *Proc. of the 2000 IEEE International Symposium on Electromagnetic Compatibility*, Washington D.C., August 2000, pp. 335-338.

T. H. Hubing, T. P. Van Doren, F. Sha, J. L. Drewniak, and M. Wilhelm, "An Experimental Investigation of 4-Layer Printed Circuit Board Decoupling," *Proceedings of the 1995 IEEE International Symposium on Electromagnetic Compatibility,* Atlanta, GA, August 1995, pp. 308-312.

J. Fan, J. Drewniak, J. Knighten, N. Smith, A. Orlandi, T. Van Doren, T. Hubing and R. DuBroff, "Quantifying SMT Decoupling Capacitor Placement in DC Power-Bus Design for Multilayer PCBs," IEEE Transactions on Electromagnetic Compatibility, vol. EMC-43, no. 4, Nov. 2001, pp. 588-599.

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Power Bus Decoupling Strategy

With no power plane

- layout low-inductance power distribution
- all high-frequency decoupling is local
- size bulk decoupling to meet board requirements
- size local decoupling to meet device requirements
- two caps can be much better than one
- avoid resonances by minimizing L

References:

T. Hubing, "Printed Circuit Board Power Bus Decoupling," *LG Journal of Production Engineering*, vol. 3, no. 12, December 2000, pp. 17-20. (Korean language publication) .

T. Zeeff, T. Hubing, T. Van Doren and D. Pommerenke, "Analysis of simple two-capacitor low-pass filters," IEEE Transactions on Electromagnetic Compatibility, vol. 45, no. 4, Nov. 2003, pp. 595-601.

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Power Bus Decoupling Strategy

Low-impedance planes or traces?

- ❑ choice based on bandwidth and board complexity
- ❑ planes are not always the best choice
- ❑ it is possible to achieve good decoupling either way
- ❑ trace inductance may limit current to active devices

Planes widely spaced or closely spaced?

Do you have a BGA component with 6 or more power pins at the same voltage? If so, you probably need the closely spaced power planes.

- ❑ want local or global decoupling?
- ❑ want stripline traces?
- ❑ lower impedances obtainable with closely spaced planes

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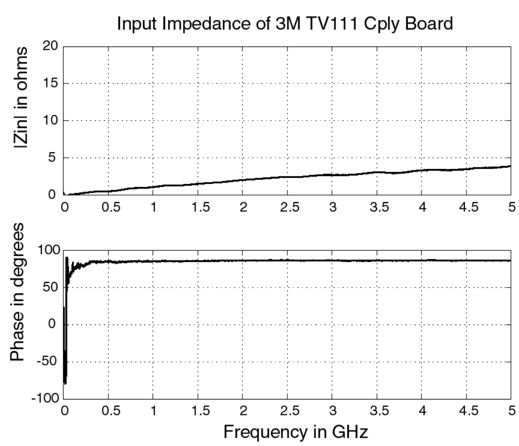
Embedded Capacitance

Input impedance of a populated 2” x 3” board with a plane separation of about 5 microns



You don’t need local high-frequency decoupling.

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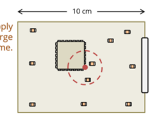
Decoupling Myths

Decoupling Myth

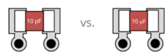
In order to be effective, capacitors must be located within a radius of the active device equal to the distance a wave can travel in the transition time of the circuitry.

While technically true, on boards with closely spaced planes (where this rule is normally applied) none of the capacitors on the board can typically respond within the transition time of the circuitry no matter where they are located.

All the capacitors on this board supply approximately the same amount of charge regardless of the circuit transition time.



Decoupling Myth



Smaller valued capacitors (i.e.; 10 pF) respond faster than higher valued capacitors.

The ability of a capacitor to supply current quickly is determined by its mounted inductance. The value of the capacitance only affects its ability to respond over longer periods of time. For a given value of inductance, higher valued capacitors are more effective for decoupling.

Use capacitors with the largest nominal value for a given package size and voltage rating.

Decoupling Myth

It is advantageous to alternate the polarity of decoupling capacitors so that the VCC connection of one capacitor is close to the GND connection of another capacitor.

This is proposed as a method for reducing the connection inductance by taking advantage of flux cancellation in the via connections of adjacent capacitors. It is effective only when the connection inductance associated with the PCB vias dominates the overall connection inductance. This should never be the case in a well-designed board.

Unless the power planes are buried deep inside the stack-up, there is very little to be gained by alternating the polarity of the decoupling capacitor vias.

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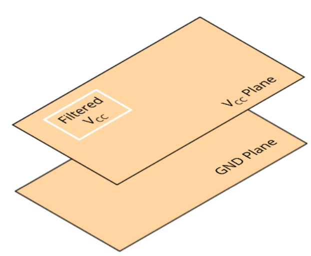
Isolating PLLs and Other Sensitive Devices

- If the PLL has one VCC pin, connect a filtered trace from the VCC plane to the pin.
- If the device has several VCC pins, it is ok to create an island in the VCC plane and filter the connection from the VCC plane to the island.
- NEVER filter the GND connection to the PLL.
- NEVER create an island in the board's GND plane.



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PCB Decoupling Summary

- Correct decoupling strategy depends on whether the board has power planes; and what the spacing between those planes is.
- Minimizing the connection inductance of decoupling capacitors is always important for high-frequency decoupling.
- Decoupling capacitors on boards with power planes should never have connecting traces and should never share a via with another decoupling capacitor.
- It is ok to filter the power connection, but never filter the ground connection.

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Electromagnetic Compatibility Principles and Design

Power Electronics Design for EMC

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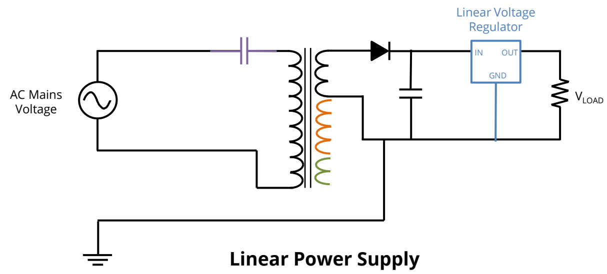
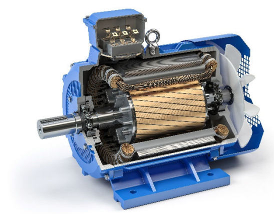
Linear Power Electronic Circuits



Linear Power Supply



Induction Motor

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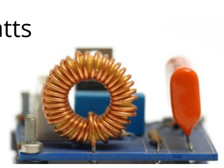
Switching Power Electronic Circuits

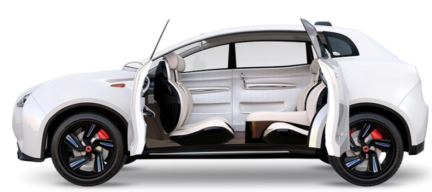
Voltage Doublers / Charge Pumps
volts
watts

DC-to-DC Converters
volts
watts

Small Motor Drives / Power Inverters
tens of volts
tens to hundreds of watts



Automotive Motor Drives
hundreds of volts
kilowatts



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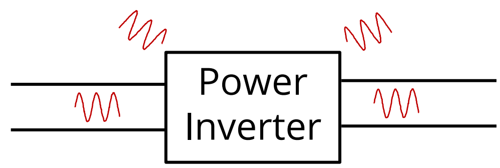
Coupling Mechanisms

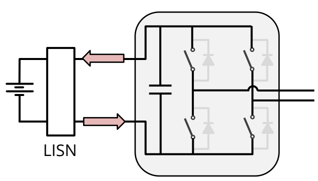
Interference problems can occur when noise from the switching power circuits couple to circuits or antenna structures that are not part of the power circuitry itself!

There are only 4 EM coupling mechanisms!

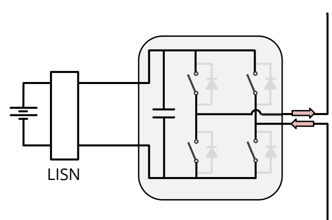
- Conducted Coupling
- Electric Field Coupling
- Magnetic Field Coupling
- Radiation Coupling



Conducted Coupling from Power Circuits



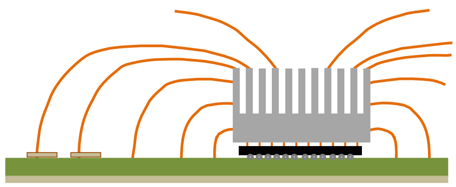
Switching Noise
Conducted on Input



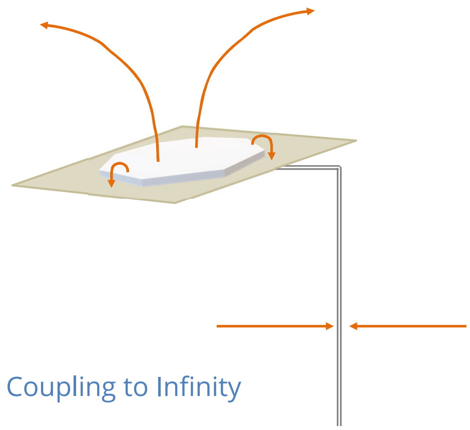
Switching Noise
Conducted on Output

Electric-Field Coupling from Power Circuits

Time domain: Proportional to $\partial V / \partial t$
Frequency domain: Proportional to ωV



Coupling to Nearby Traces or Circuits



Coupling to Infinity

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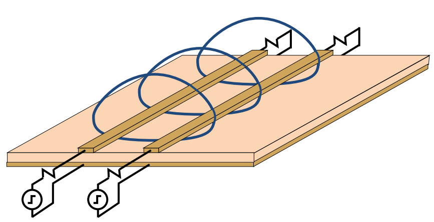
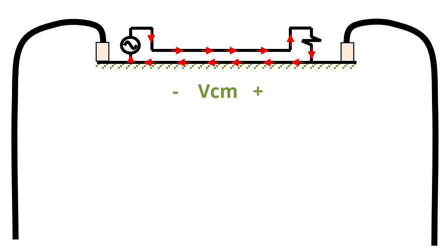
Magnetic-Field Coupling from Power Circuits

Time domain: Proportional to $\partial I / \partial t$
Frequency domain: Proportional to ωI



Coupling to Nearby Traces or Circuits



Coupling to Cables

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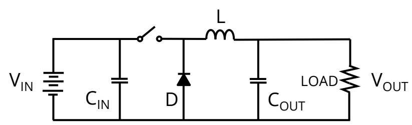
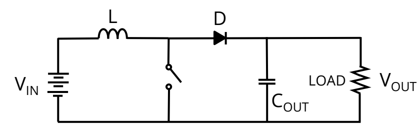
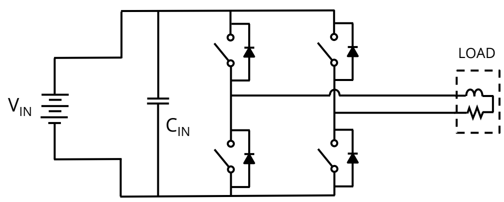
Overview of Power Electronic Circuit Topologies



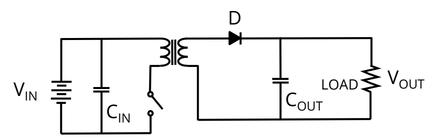
DC-DC Buck Converter



DC-DC Boost Converter



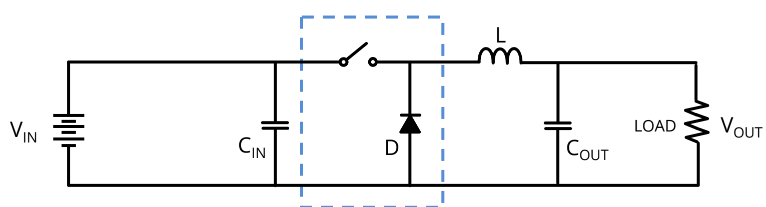
DC-AC Inverter



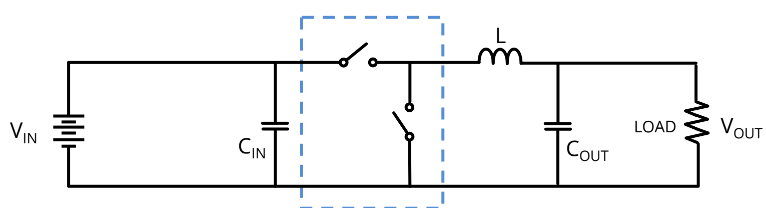
Flyback Converter

Buck Converter Topology

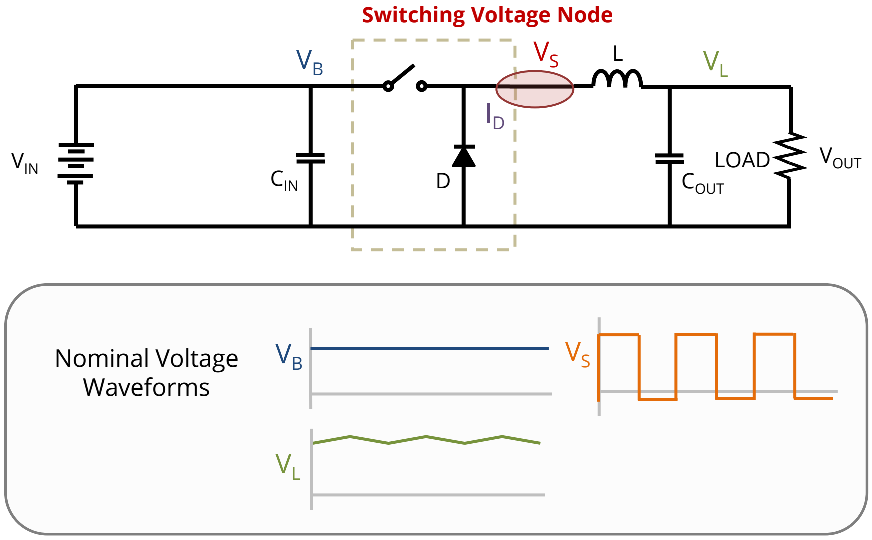
Asynchronous



Synchronous



Buck Converter Topology



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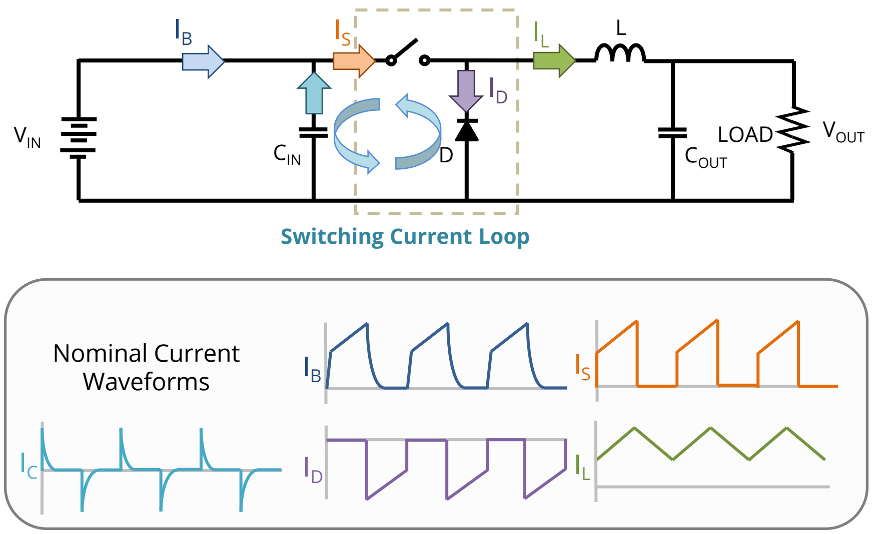
Buck Converter Topology



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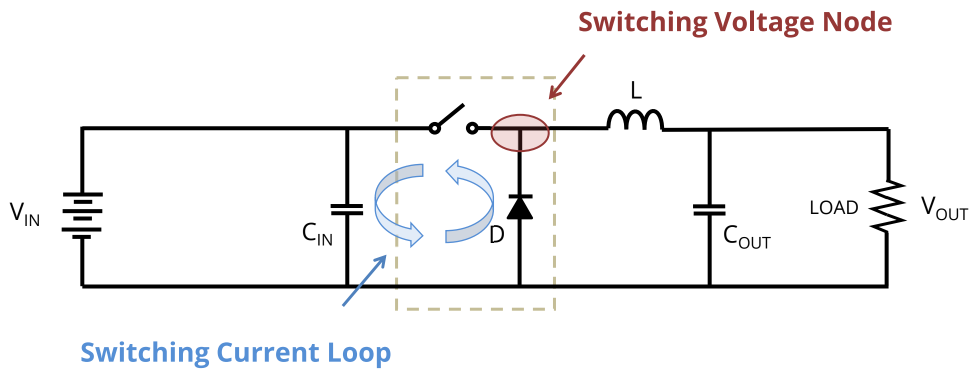
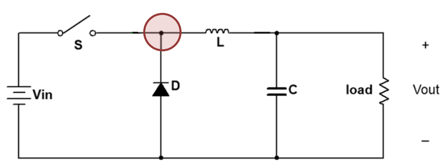
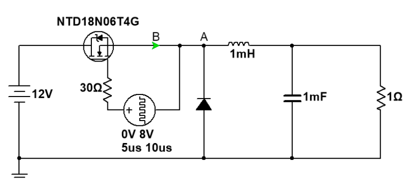
Buck Converter Topology



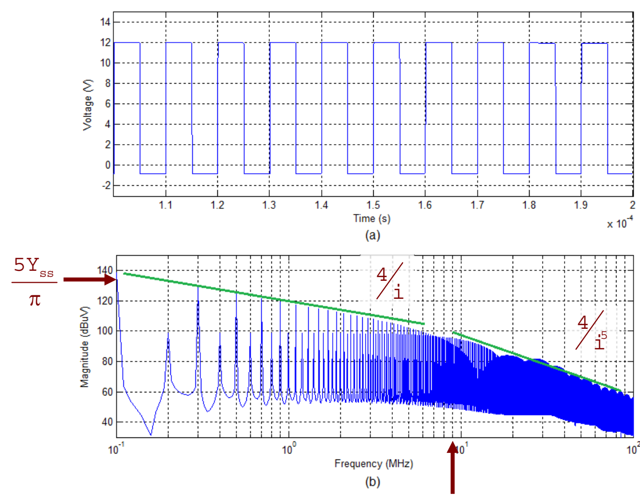
Characterizing the Source



DC-DC buck converter schematic

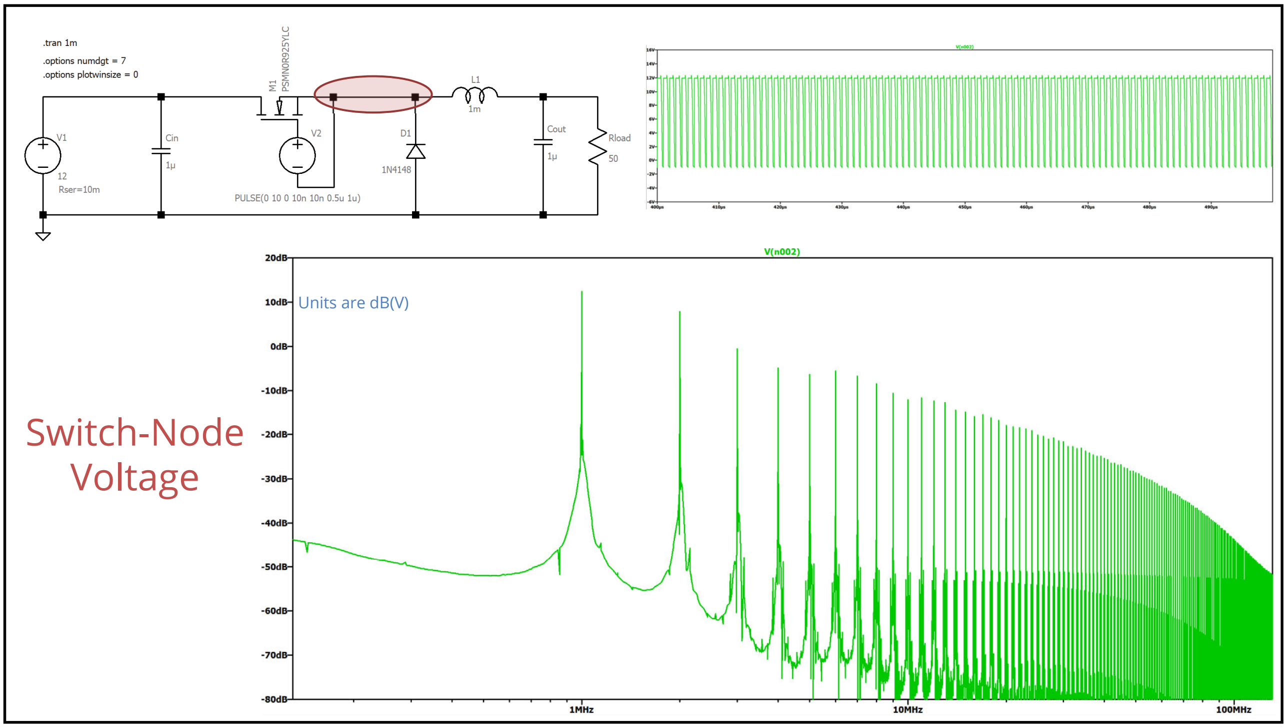


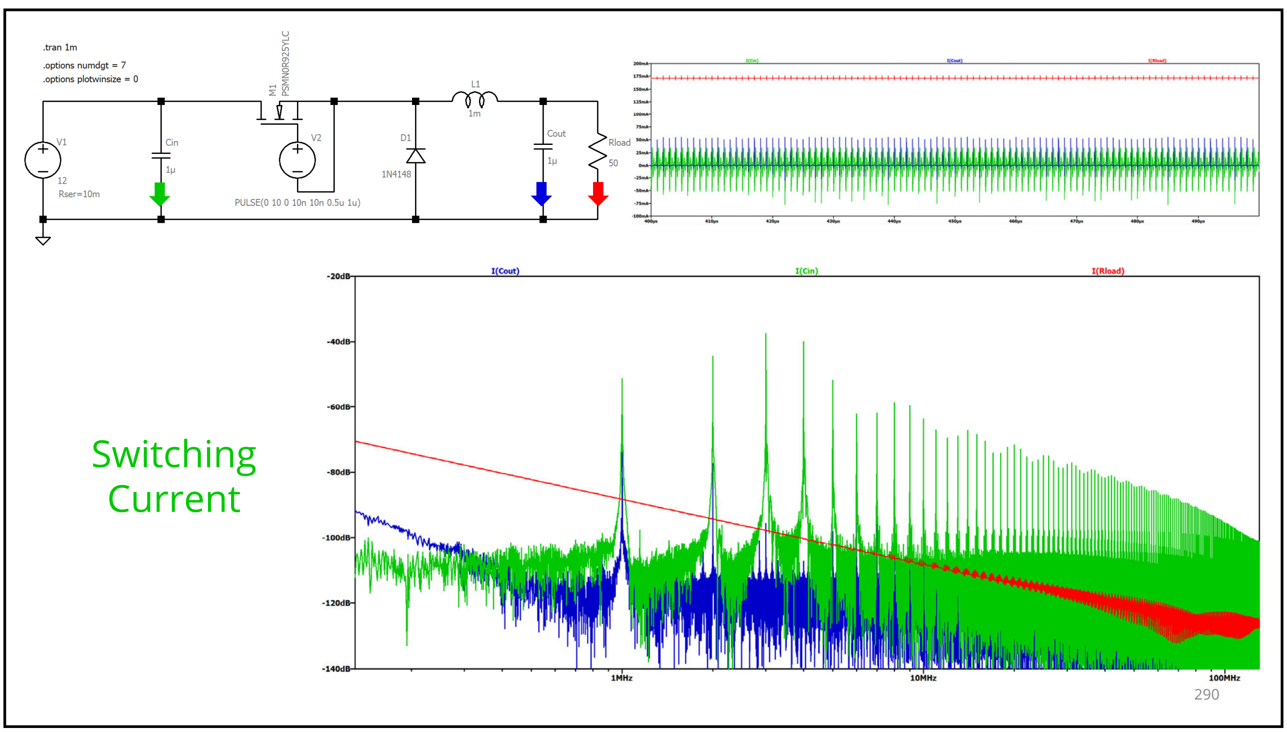
DC-DC buck converter model for simulation

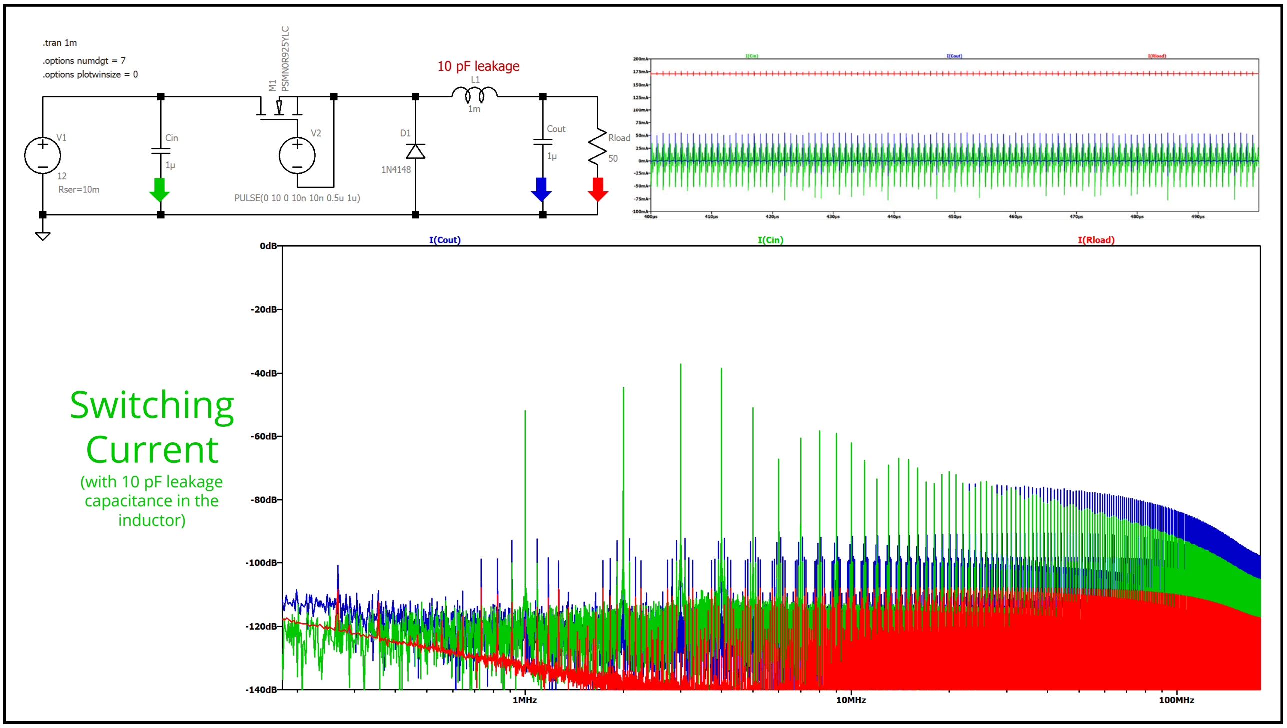


Voltage waveform at node A:
(a) time domain
(b) frequency domain

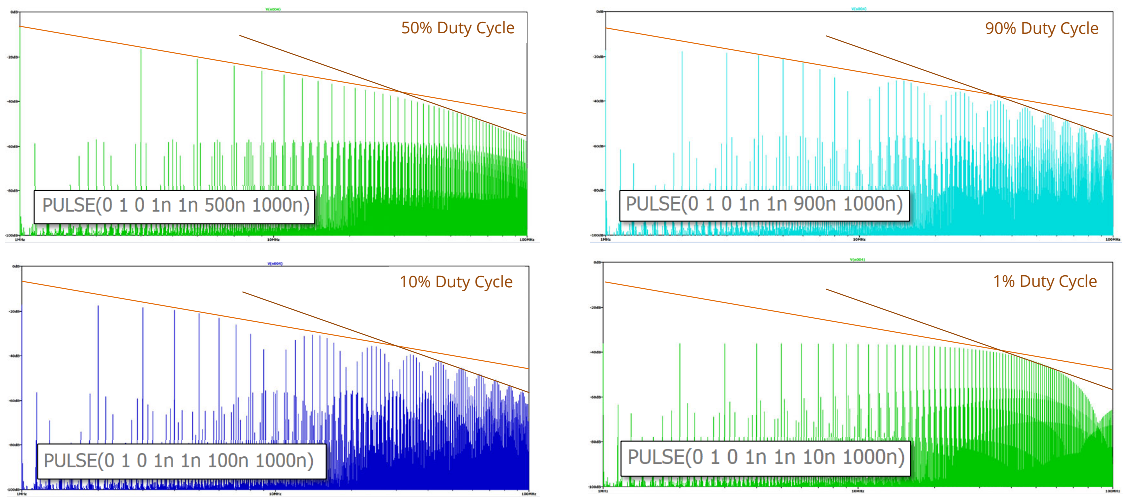
$\frac{4}{\pi w_u}$ $t_r = 0.4\ \mu s$


.tran 1m
.options numdgt = 7
.options plotwinsize = 0
M1
PSMN0R925YLC
L1
1m
V1
12
Rser=10m
Cin
1µ
V2
PULSE(0 10 0 10n 10n 0.5u 1u)
D1
1N4148
Cout
1µ
Rload
50
V(n002)
Units are dB(V)
Switch-Node Voltage
1MHz
10MHz
100MHz


.tran 1m
.options numdgt = 7
.options plotwinsize = 0
M1
PSMN0R925YLC
L1
1m
V1
12
Rser=10m
Cin
1µ
V2
PULSE(0 10 0 10n 10n 0.5u 1u)
D1
1N4148
Cout
1µ
Rload
50
I(Cout)
I(Cin)
I(Rload)
Switching Current
1MHz
10MHz
100MHz
290



Effect of Pulse Width on Frequency Content



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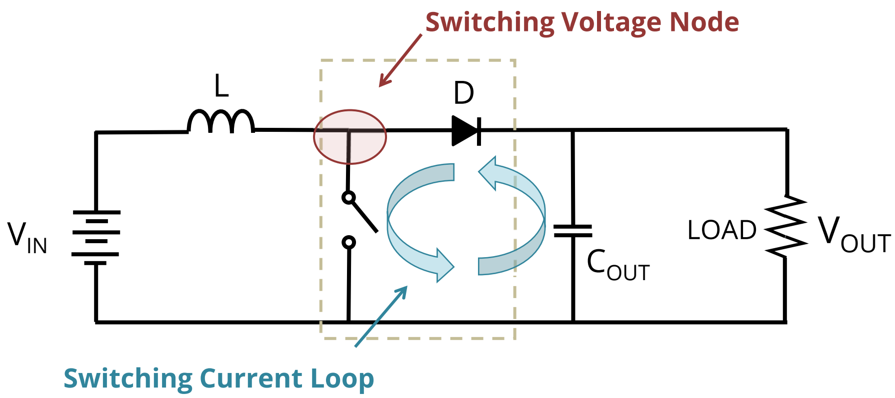
Boost Converter Topology



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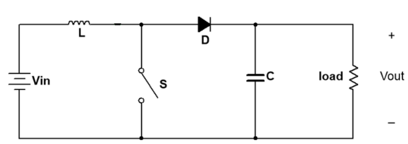
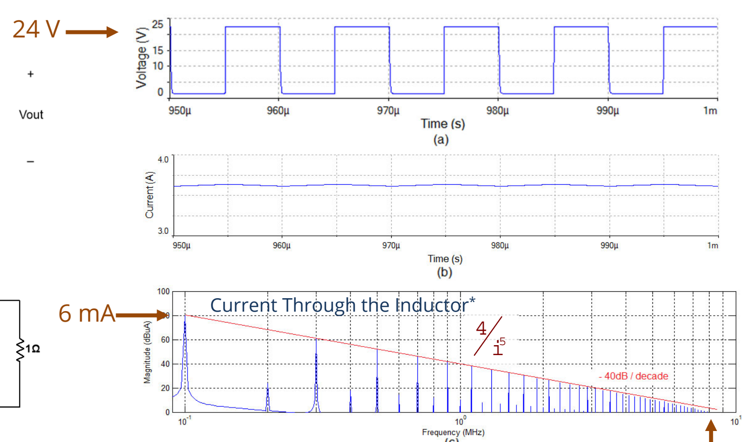
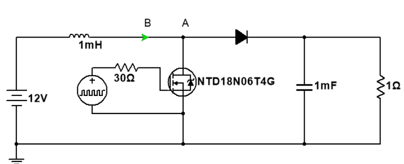
Characterizing the Source



DC-DC boost converter schematic





DC-DC boost converter model for simulation

Waforms:

(a) voltage at node A
(b) current at location B
(c) MOSFET current spectrum

$\frac{4}{\pi w_u}$

* Note that current in the switching current loop is 60 mA peak and falls off proportional to frequency until $1/\pi t_r$.

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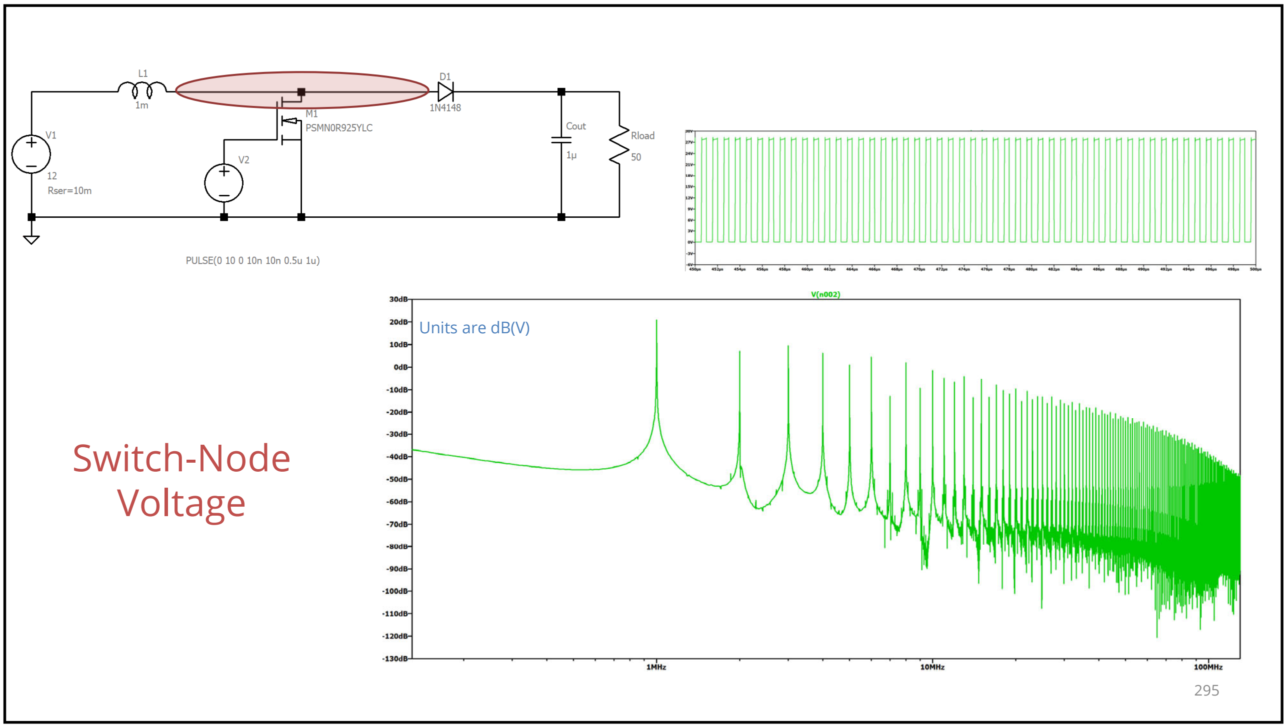
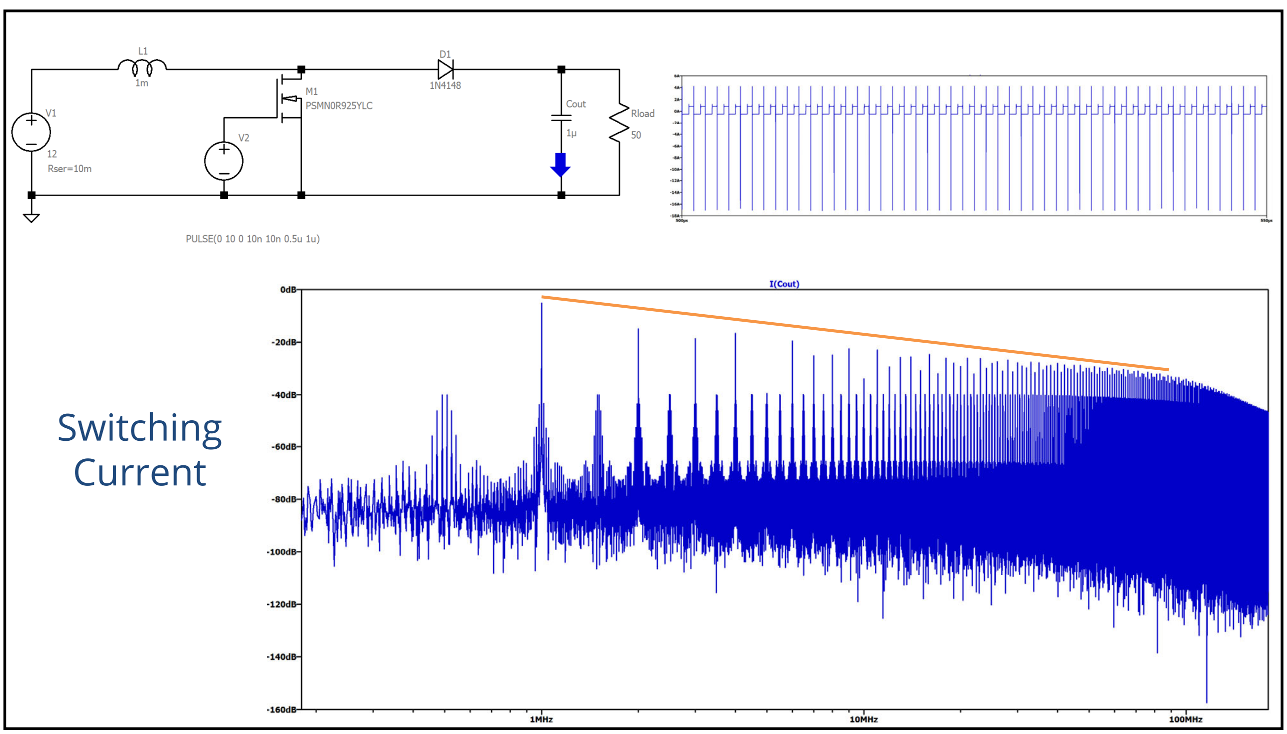
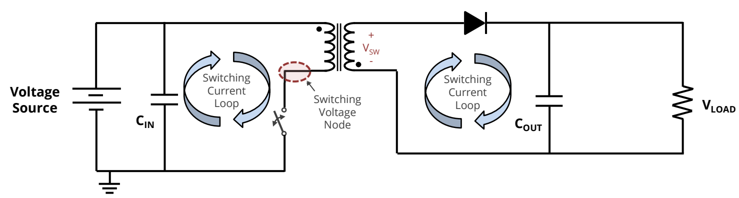
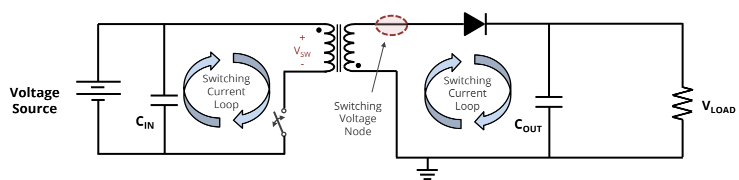

L1
1m
D1
1N4148
M1
PSMN0R925YLC
V1
12
Rser=10m
V2
Cout
1µ
Rload
50
PULSE(0 10 0 10n 10n 0.5u 1u)
V(n002)
Units are dB(V)
Switch-Node Voltage
1MHz
10MHz
100MHz
295


L1
1m
D1
1N4148
M1
PSMN0R925YLC
V1
12
Rser=10m
V2
Cout
1µ
Rload
50
PULSE(0 10 0 10n 10n 0.5u 1u)
I(Cout)
Switching Current
0dB
-20dB
-40dB
-60dB
-80dB
-100dB
-120dB
-140dB
-160dB
1MHz
10MHz
100MHz

Flyback Converter

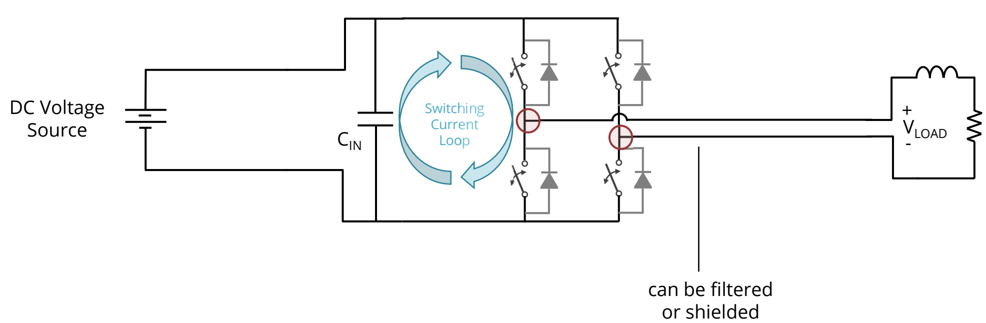


Flyback Converter (primary grounded)

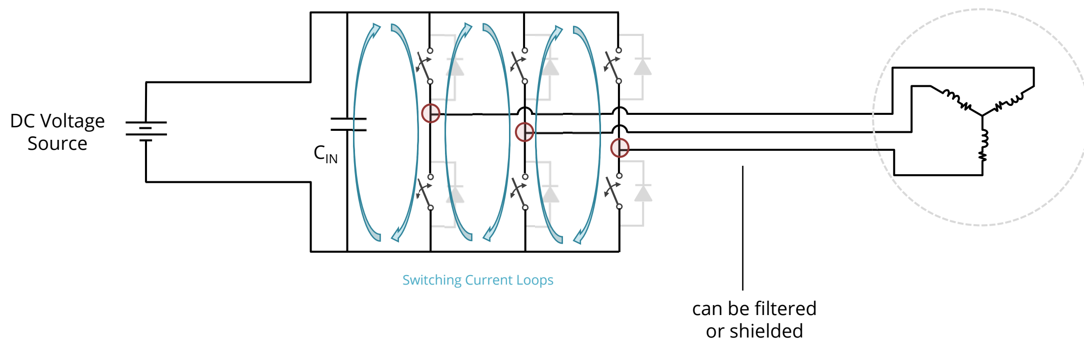


Flyback Converter (secondary grounded)

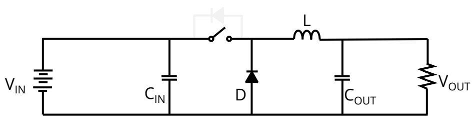
Single-Phase Inverter or H-Bridge



Three-Phase Inverter

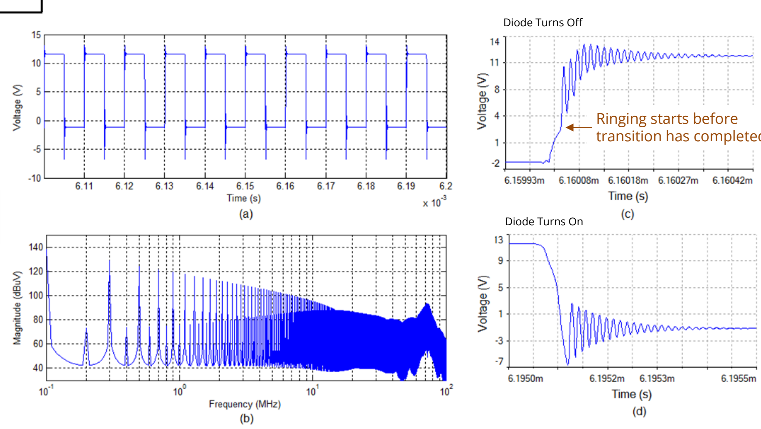


Key EMC Compliance Issues



Ringing Current

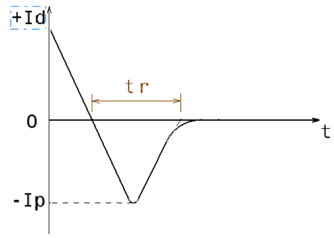
Ringing in the switching waveform adds to the switching CM voltage noise.



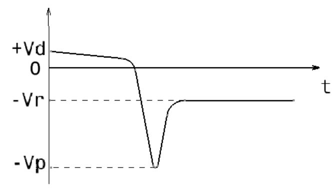
Diode Reverse Recovery

In contrast to an ideal diode in which the current would stay at zero, the current in a real diode increases in the opposite direction to a peak value of I_p, and returns to zero only after a time, t_r. t_r is called the reverse recovery time. As a result, the voltage across the diode will have a negative spike, V_p, before it settles at V_r.

The reverse recovery time of a diode can be of the order of nanoseconds and the negative current spike can be very high. These narrow current spikes produce wide band noise. In power converters, this wideband noise can enhance the ringing in the voltage and current waveforms due to the parasitic L and C in the circuit.

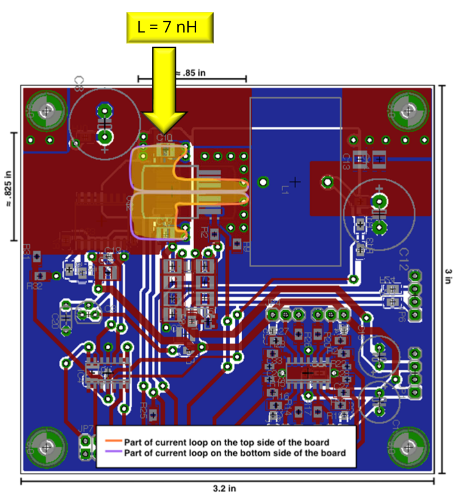


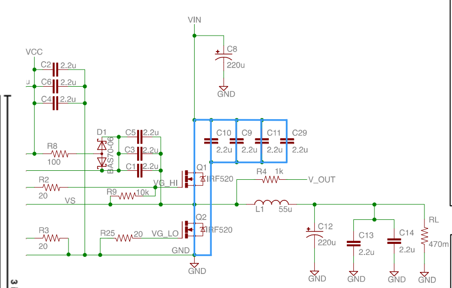
(a)

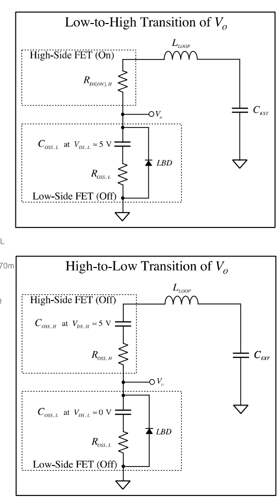


(b)

Identification of Ringing Loop Inductance



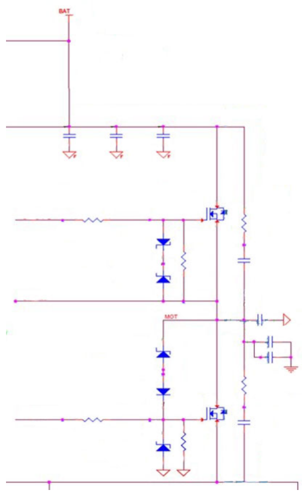


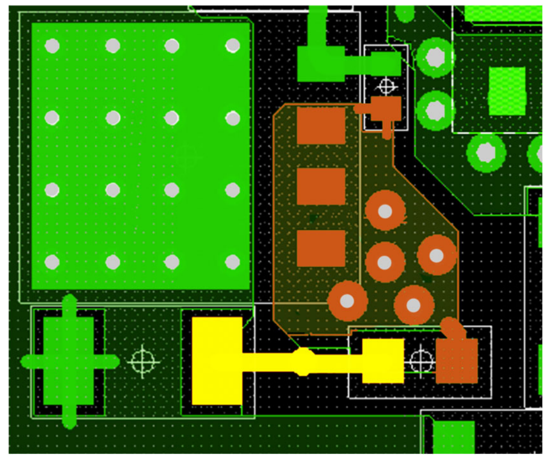


Ringing Frequency: $f_0 = \frac{1}{2\pi\sqrt{LC}}$

Q Factor: $Q = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{1}{2\zeta} = \frac{\pi f_0}{\alpha}$

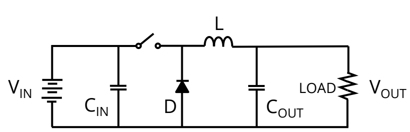
Snubber Circuits





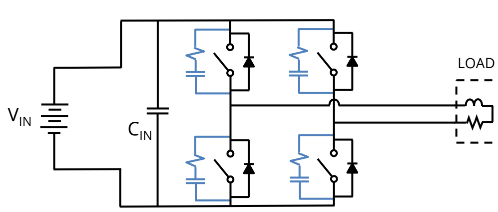
Snubber Circuits

Don't put snubber circuits on low-power or medium-power DC-to-DC converters.



Just keep the voltage switching node and the switching current loop small!

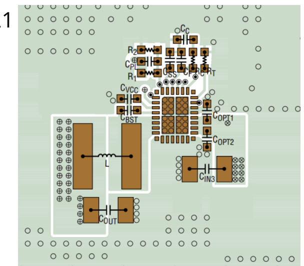
Do put snubber circuits on medium-power to high-power DC-to-AC inverters.



When required to prevent excessive ringing!

New Technologies

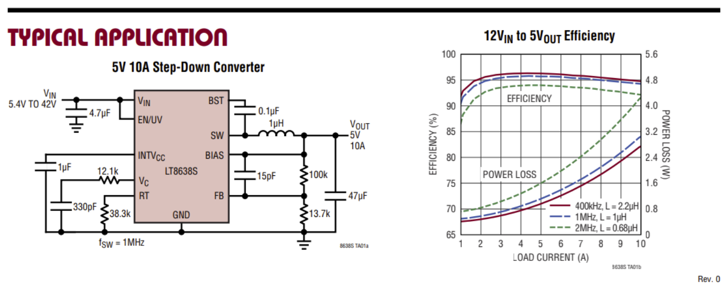
4/21



Analog Devices LT8638S (Buck Converter)

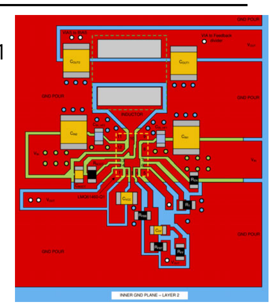
- 5V from 2.8 – 42 V
- 10 A
- 1 – 2 MHz
- Silent Switcher® Architecture

- Input Capacitance in package
- Optional Spread Spectrum



New Technologies

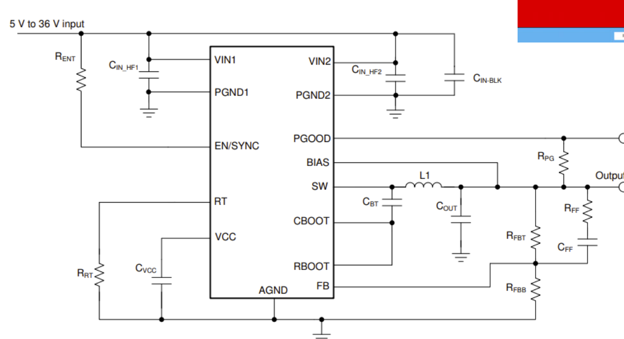
1/21



Texas Instruments LMQ61460-Q1 (Buck Converter)

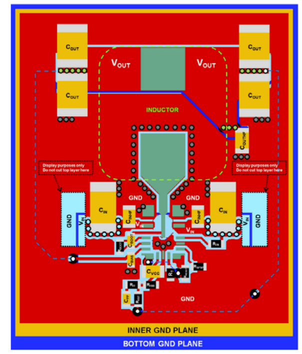
- 3 – 36 V from 5 - 36 V
- 6 A
- 0.2 – 2 MHz
- “Low EMI”

- Input Capacitance in package
- Optional Spread Spectrum



New Technologies

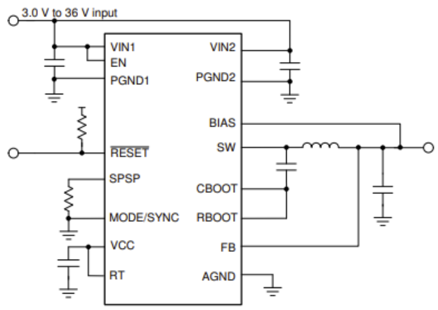
11/21



Texas Instruments LM62460 (Buck Converter)

- 3 – 36 V from 3 - 36 V
- 6 A
- 0.2 – 2.2 MHz
- "Low EMI symmetrical pinout"

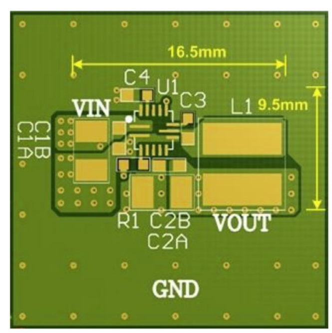
- Adjustable SW node rise time
- Configurable Spread Spectrum



Simplified Schematic

New Technologies

3/19

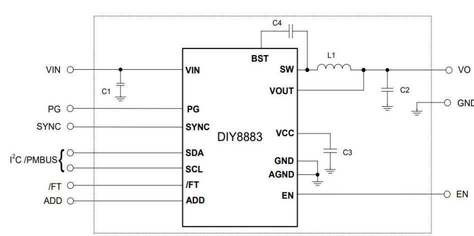


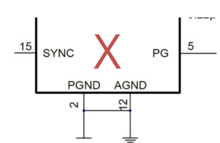
MPS DIY8883 (Synchronous Buck Converter)

- 0.6 – 12 V from 3.5 – 45 V
- 3 A
- 0.2 – 2.2 MHz

- Programmable Slew Rate
- "Frequency Dithering"

TYPICAL APPLICATION



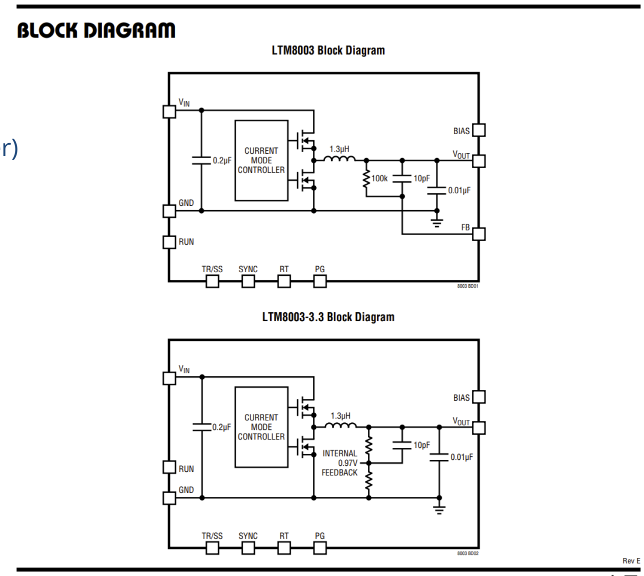


New Technologies

Analog Devices LTM8003 (Buck Converter)

- 5V from 7 – 40 V
- 3.5 A
- 1 – 3 MHz
- Silent Switcher® Architecture

- Input Capacitance in package
- Inductor in package



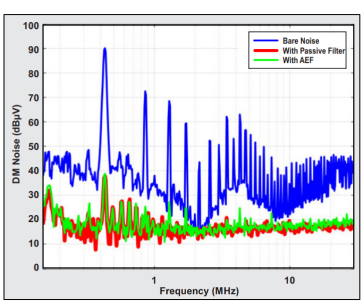
Active EMI Filtering

Texas Instruments
www.ti.com
LM25149-Q1
SNVSBV6A – DECEMBER 2020 – REVISED APRIL 2021

9.2 Typical Applications

9.2.1 Design 1 – High Efficiency 2.1 MHz Buck Regulator

Figure 9-5 shows the schematic diagram of a single-output synchronous buck regulator with output voltage of 5 V and a rated load current of 8 A. In this example, the target half-load and full-load efficiencies are 93.5% and 92.5%, respectively, based on a nominal input voltage of 12 V that ranges from 5.5 V to 36 V. The switching frequency is set at 2.1 MHz by resistor R_{RT}. The 5-V output is connected to VCCX to reduce IC bias power dissipation and improve efficiency. An output voltage of 3.3 V is also feasible simply by connecting FB to VDDA (tie VCCX to GND in this case).



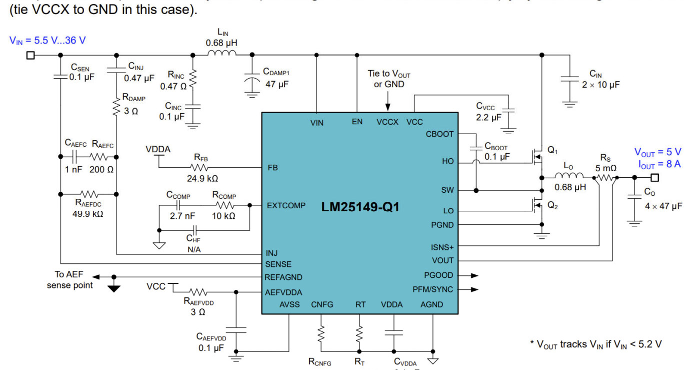
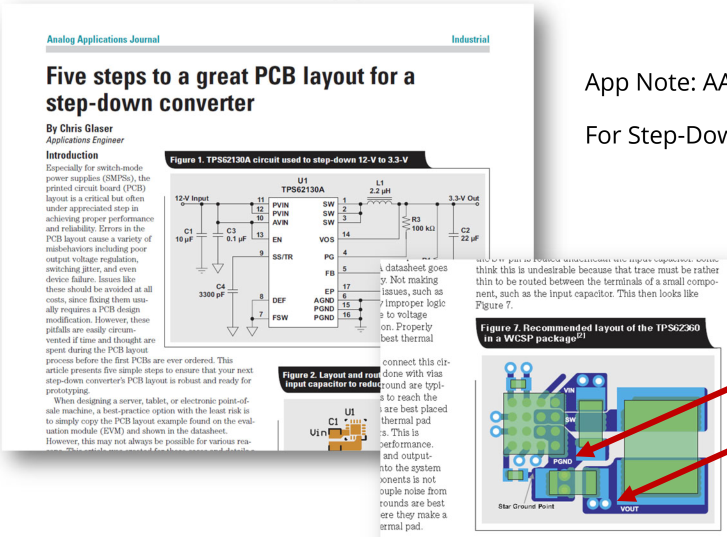


Figure 9-5. Application Circuit 1 With LM25149-Q1 Buck Regulator at 2.1 MHz

Texas Instruments Application Note



App Note: AAJ 1Q 2015

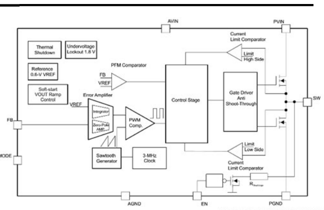
For Step-Down Converters

Note that HF current will not flow on isolated PGND. Path of least inductance takes it back to main ground plane.

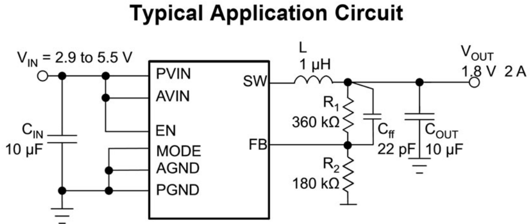
Single-point current return?!!

TLV62065 DC/DC Buck Converter (Data Sheet)

Automotive 2.9V to 5.5V, 3 MHz, 2A



Typical Application Circuit



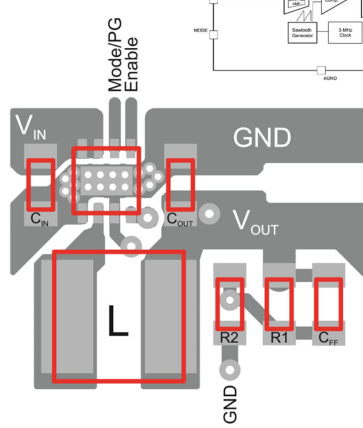
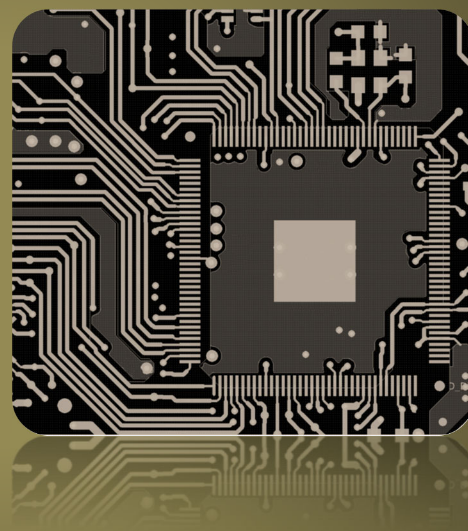


Figure 24. PCB Layout

Be sure that vias to GND and any voltage planes are adjacent to capacitor mounting pads!

Electromagnetic Compatibility Principles and Design

Key System-Level Design Considerations



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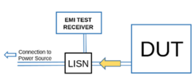


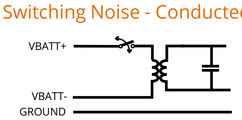
Conducted Emissions

- 1 HF GND
- SMPS Layout
- Filter Design
- Filter Layout
- Balance Control
- Transition Times
- Adequate Decoupling

EMC Requirements and Key Design Considerations

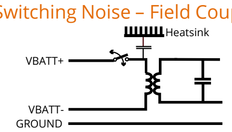
Common Sources of Conducted EMI

Switching Noise - Conducted



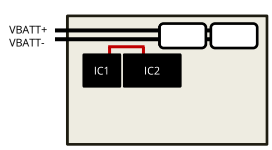
- Noise produced directly by switching on the power input
- Mitigation Option 1: Appropriate Filtering
- Mitigation Option 2: Control parameters of the switching

Switching Noise – Field Coupled



- Noise voltage drives capacitance to chassis or earth
- Mitigation Option 1: Reduce capacitance
- Mitigation Option 2: Appropriate Filtering
- Mitigation Option 3: Control parameters of the switching

Switching Noise Coupled to a Power Line



- Noise coupled directly to power input traces or components
- Mitigation Option 1: Reduce the coupling
- Mitigation Option 2: Appropriate Filtering
- Mitigation Option 3: Control parameters of the switching

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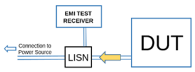
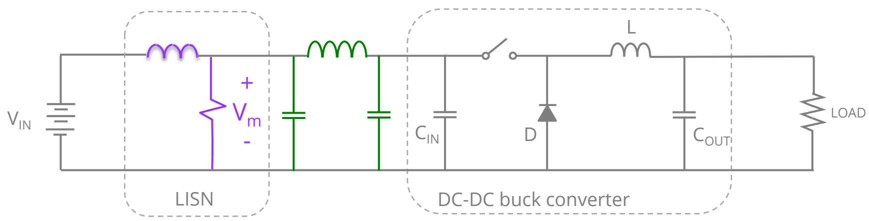
EMC Requirements and Key Design Considerations



Conducted Emissions

- 1 HF GND
- SMPS Layout
- Filter Design
- Filter Layout
- Balance Control
- Transition Times
- Adequate Decoupling



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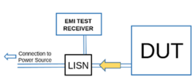
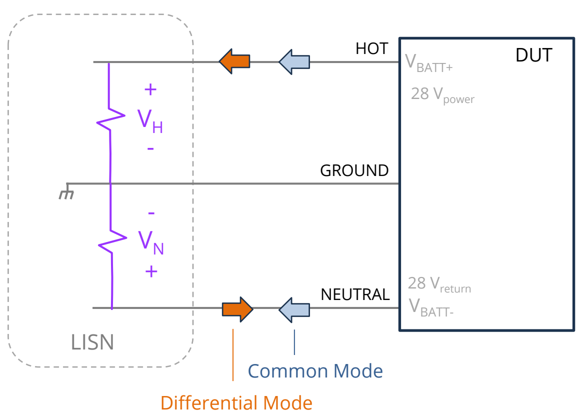
EMC Requirements and Key Design Considerations



Conducted Emissions

- 1 HF GND
- SMPS Layout
- Filter Design
- Filter Layout
- Balance Control
- Transition Times
- Adequate Decoupling

Two-Phase Power, Two Propagation Modes



$$V_{CM} = \frac{V_H + V_N}{2}$$

$$V_{DM} = V_H - V_N$$

$$V_H = V_{CM} + \frac{V_{DM}}{2}$$

$$V_N = V_{CM} - \frac{V_{DM}}{2}$$

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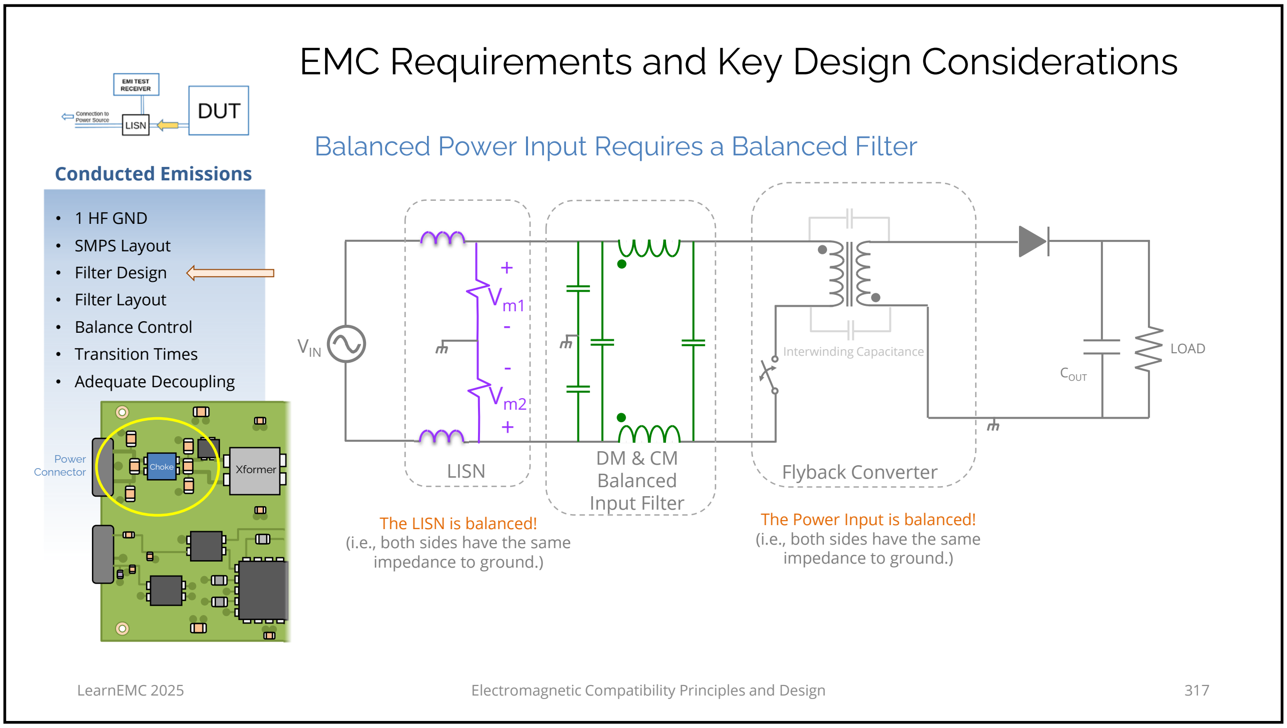
EMC Requirements and Key Design Considerations
EMI TEST RECEIVER
Connection to Power Source
LISN
DUT
Conducted Emissions
1 HF GND
SMPS Layout
Filter Design
Filter Layout
Balance Control
Transition Times
Adequate Decoupling
Power Connector
Choke
Xformer
Balanced Power Input Requires a Balanced Filter
VIN
+
Vm1
-
-
Vm2
+
LISN
DM & CM Balanced Input Filter
Interwinding Capacitance
Flyback Converter
COUT
LOAD
The LISN is balanced!
(i.e., both sides have the same impedance to ground.)
The Power Input is balanced!
(i.e., both sides have the same impedance to ground.)
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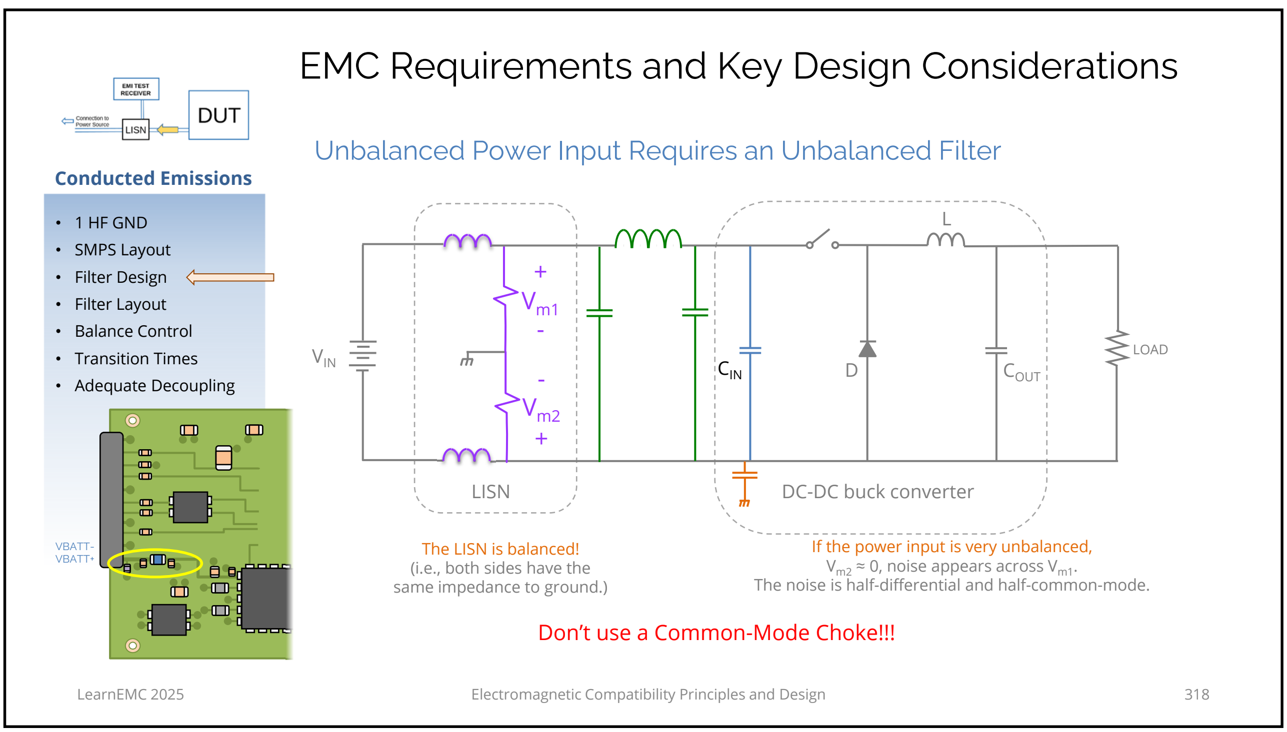
Electromagnetic Compatibility Principles and Design
317


EMC Requirements and Key Design Considerations
EMI TEST RECEIVER
Connection to Power Source
LISN
DUT
Conducted Emissions
1 HF GND
SMPS Layout
Filter Design
Filter Layout
Balance Control
Transition Times
Adequate Decoupling
VBATT-
VBATT+
Unbalanced Power Input Requires an Unbalanced Filter
VIN
+
Vm1
-
-
Vm2
+
LISN
L
CIN
D
COUT
LOAD
DC-DC buck converter
The LISN is balanced!
(i.e., both sides have the same impedance to ground.)
If the power input is very unbalanced,
Vm2 ≈ 0, noise appears across Vm1.
The noise is half-differential and half-common-mode.
Don't use a Common-Mode Choke!!!
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Electromagnetic Compatibility Principles and Design
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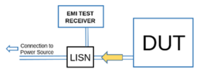
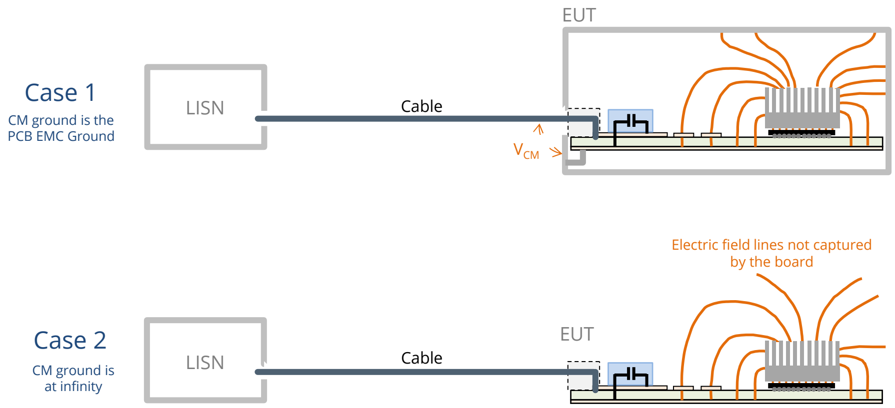
EMC Requirements and Key Design Considerations



Conducted Emissions

- 1 HF GND
- SMPS Layout
- Filter Design
- Filter Layout
- Balance Control
- Transition Times
- Adequate Decoupling

Electric-Field Coupling



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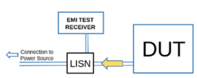
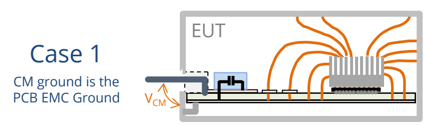
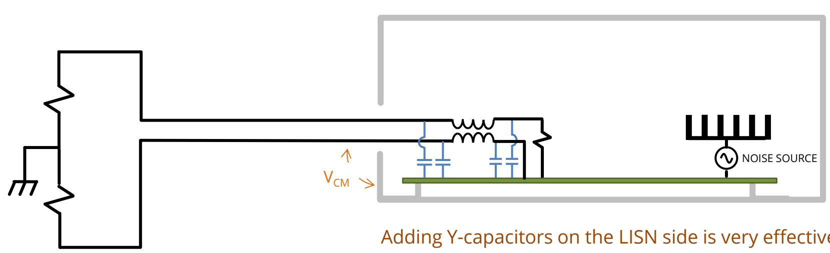
EMC Requirements and Key Design Considerations



Conducted Emissions

- 1 HF GND
- SMPS Layout
- Filter Design
- Filter Layout
- Balance Control
- Transition Times
- Adequate Decoupling





Adding Y-capacitors on the LISN side is very effective.

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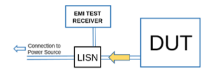
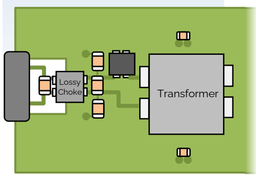
EMC Requirements and Key Design Considerations

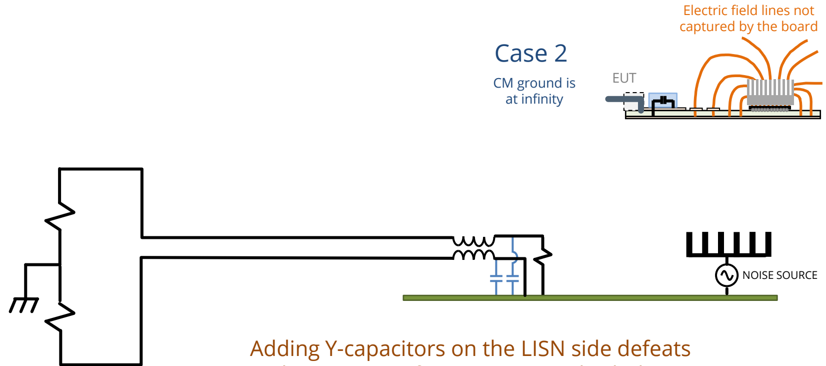


Conducted Emissions

- 1 HF GND
- SMPS Layout
- Filter Design
- Filter Layout
- Balance Control
- Transition Times
- Adequate Decoupling



Balanced Filter (small board with no chassis)



Adding Y-capacitors on the LISN side defeats the purpose of a common-mode choke!

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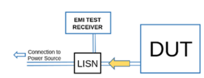
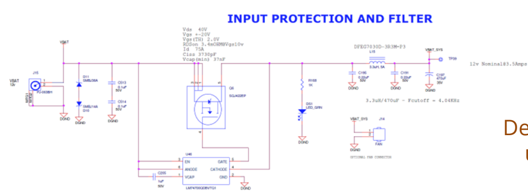
EMC Requirements and Key Design Considerations

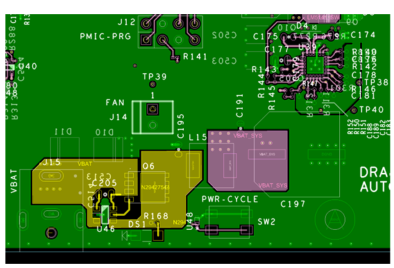


Conducted Emissions

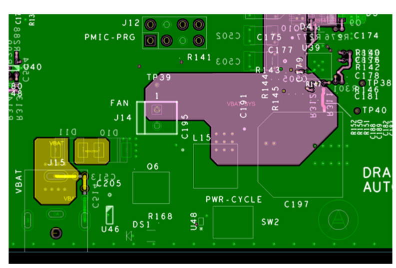
- 1 HF GND
- SMPS Layout
- Filter Design
- Filter Layout
- Balance Control
- Transition Times
- Adequate Decoupling



Design a good filter and don't unintentionally bypass it.



Top Layer



Bottom Layer

The LISN is measuring the voltage relative to CHASSIS ground. If your digital ground has a voltage relative to chassis ground, it will appear in your measurement.

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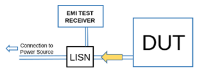
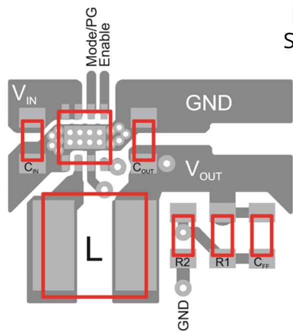


Conducted Emissions

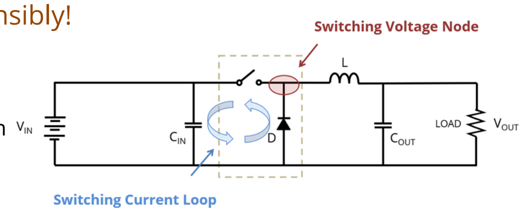
- 1 HF GND
- SMPS Layout
- Filter Design
- Filter Layout
- Balance Control
- Transition Times
- Adequate Decoupling

EMC Requirements and Key Design Considerations

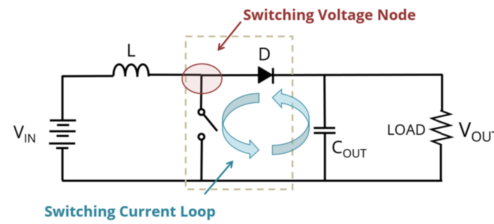
Layout out power converters sensibly!



DC-to-DC
Step Down
(Buck)



DC-to-DC
Step Up
(Boost)



Ignore bad advice in app notes!

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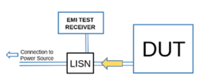
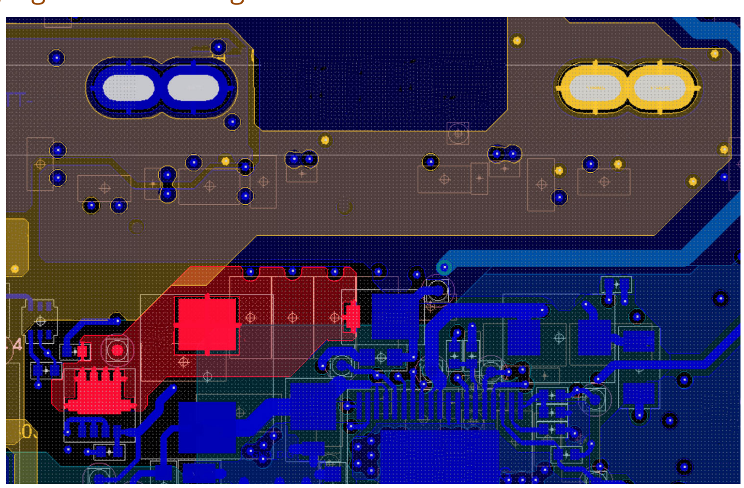


Conducted Emissions

- 1 HF GND
- SMPS Layout
- Filter Design
- Filter Layout
- Balance Control
- Transition Times
- Adequate Decoupling

EMC Requirements and Key Design Considerations

Highlight the Switching Nodes!



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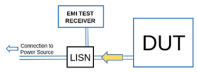
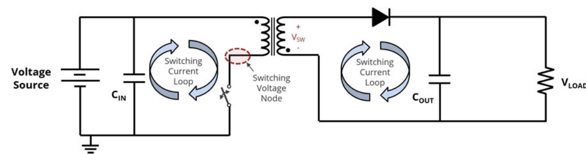
EMC Requirements and Key Design Considerations



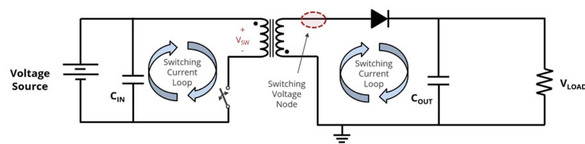
Conducted Emissions

- 1 HF GND
- SMPS Layout
- Filter Design
- Filter Layout
- Balance Control
- Transition Times
- Adequate Decoupling

Layout out flyback power converters sensibly!



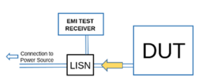
Flyback Converter (primary grounded)



Flyback Converter (secondary grounded)

Ignore bad advice in app notes!

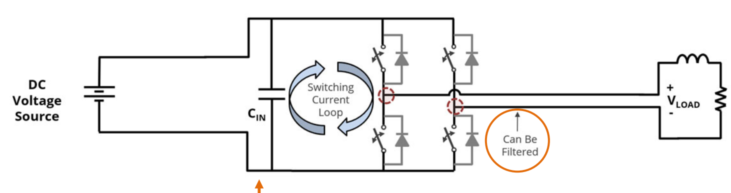
EMC Requirements and Key Design Considerations



Conducted Emissions

- 1 HF GND
- SMPS Layout
- Filter Design
- Filter Layout
- Balance Control
- Transition Times
- Adequate Decoupling

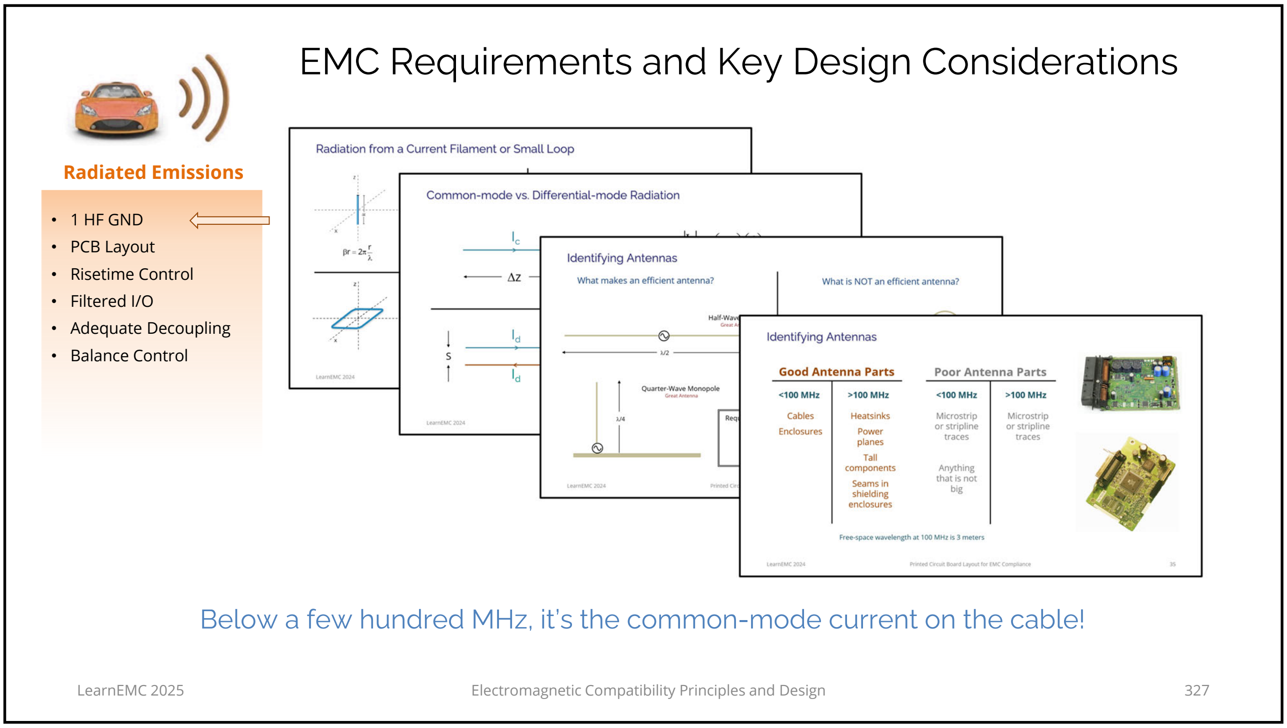
Layout out motor drivers sensibly!



H-Bridge

Don't isolate the "motor ground" from digital return unless you can show that it is necessary !

Ignore bad advice in app notes!


EMC Requirements and Key Design Considerations
Radiated Emissions
• 1 HF GND
• PCB Layout
• Risetime Control
• Filtered I/O
• Adequate Decoupling
• Balance Control
Radiation from a Current Filament or Small Loop
Common-mode vs. Differential-mode Radiation
Identifying Antennas
What makes an efficient antenna?
What is NOT an efficient antenna?
Quarter-Wave Monopole
Identifying Antennas
Good Antenna Parts
Poor Antenna Parts
<100 MHz
>100 MHz
Cables
Enclosures
Heatsinks
Power planes
Tall components
Seams in shielding enclosures
Microstrip or stripline traces
Anything that is not big
Free-space wavelength at 100 MHz is 3 meters
Below a few hundred MHz, it's the common-mode current on the cable!
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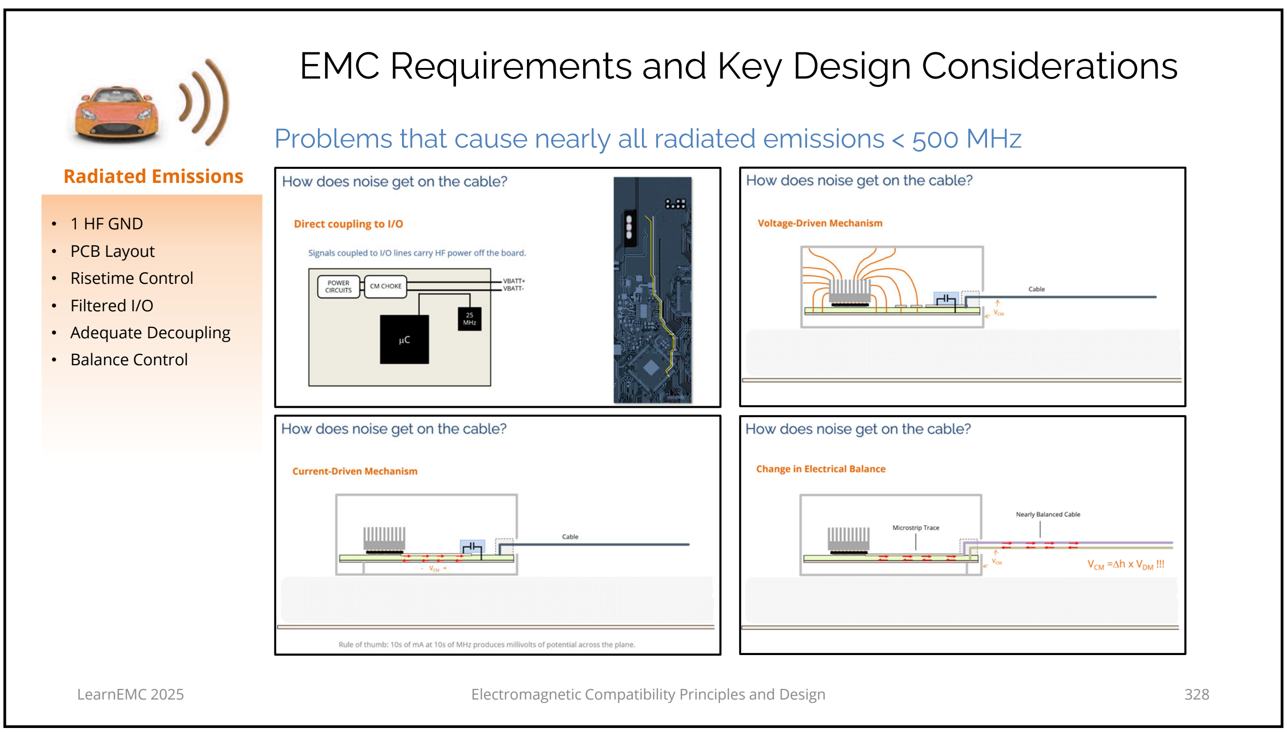
EMC Requirements and Key Design Considerations
Radiated Emissions
• 1 HF GND
• PCB Layout
• Risetime Control
• Filtered I/O
• Adequate Decoupling
• Balance Control
Problems that cause nearly all radiated emissions < 500 MHz
How does noise get on the cable?
Direct coupling to I/O
Signals coupled to I/O lines carry HF power off the board.
POWER CIRCUITS
CM CHOKE
VBATT+
VBATT-
µC
How does noise get on the cable?
Voltage-Driven Mechanism
Cable
How does noise get on the cable?
Current-Driven Mechanism
Cable
Rule of thumb: 10s of mA at 10s of MHz produces millivolts of potential across the plane.
How does noise get on the cable?
Change in Electrical Balance
Microstrip Trace
Nearly Balanced Cable
$V_{CM} = \Delta h \times V_{DM}$!!!
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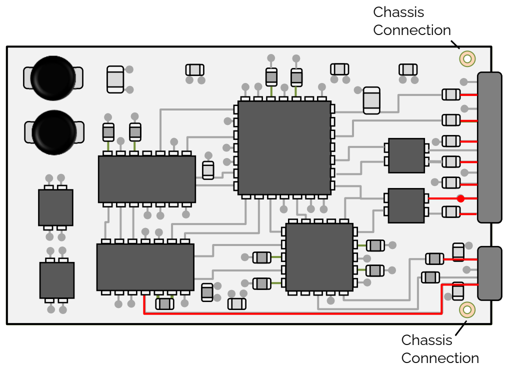
EMC Requirements and Key Design Considerations

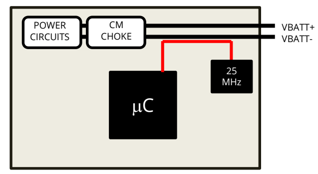
Radiated Emissions

- 1 HF GND
- PCB Layout
- Risetime Control
- Filtered I/O
- Adequate Decoupling
- Balance Control



Direct Coupling to I/O

Signals coupled to I/O lines carry HF power off the board.



Key Layout Techniques

- Highlight every net on a connector pin.
- Look for unintentional coupling to high-frequency traces.
- Follow the trace from the connector to each series termination.
- Reroute or terminate traces as necessary.

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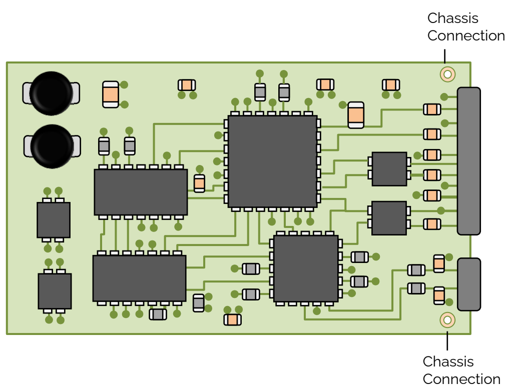
EMC Requirements and Key Design Considerations

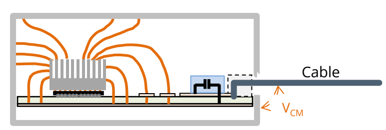
Radiated Emissions

- 1 HF GND
- PCB Layout
- Risetime Control
- Filtered I/O
- Adequate Decoupling
- Balance Control



Voltage-Driven Mechanism

Electric-field lines drive the chassis or infinity relative to cable



Key Layout Techniques

- Keep heatsinks and switching nets small relative to the board size.
- Filter each I/O trace with series resistance and/or parallel capacitance to chassis ground.
- Provide a good low-inductance connection to chassis.

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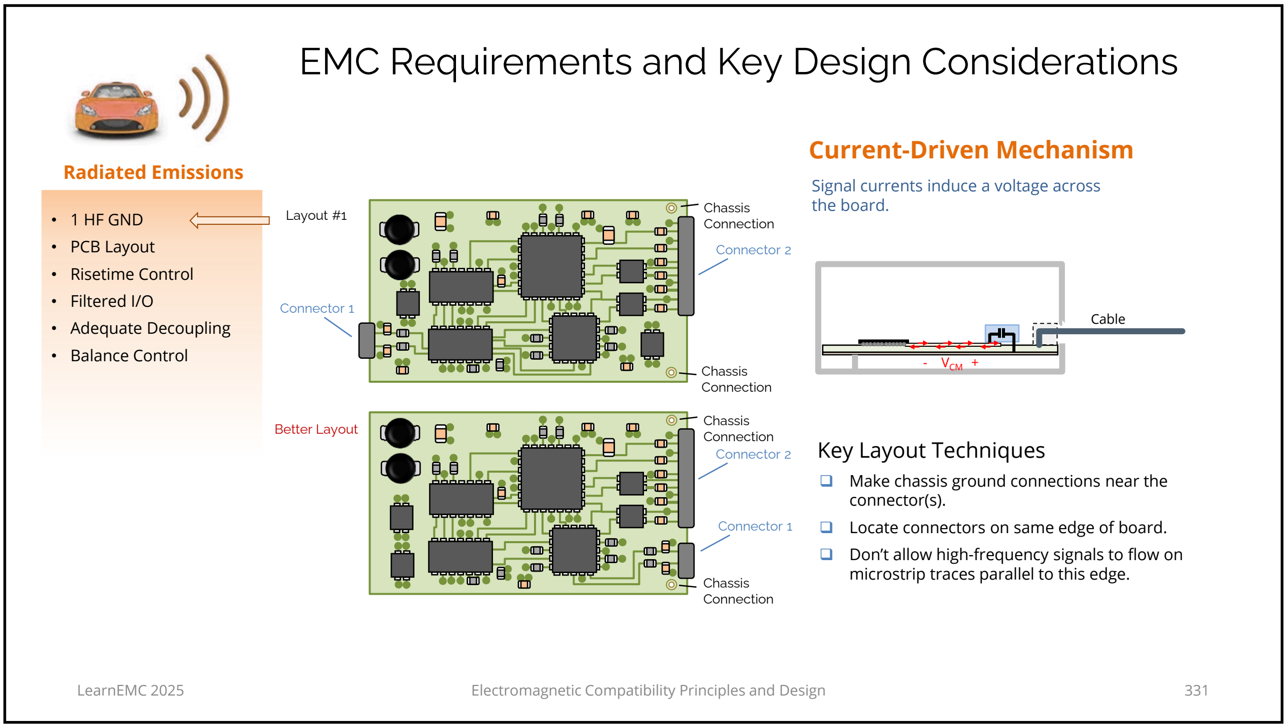
EMC Requirements and Key Design Considerations
Radiated Emissions
• 1 HF GND
• PCB Layout
• Risetime Control
• Filtered I/O
• Adequate Decoupling
• Balance Control
Layout #1
Connector 1
Connector 2
Chassis Connection
Chassis Connection
Better Layout
Chassis Connection
Connector 2
Connector 1
Chassis Connection
Current-Driven Mechanism
Signal currents induce a voltage across the board.
Cable
- VCM +
Key Layout Techniques
❑ Make chassis ground connections near the connector(s).
❑ Locate connectors on same edge of board.
❑ Don't allow high-frequency signals to flow on microstrip traces parallel to this edge.
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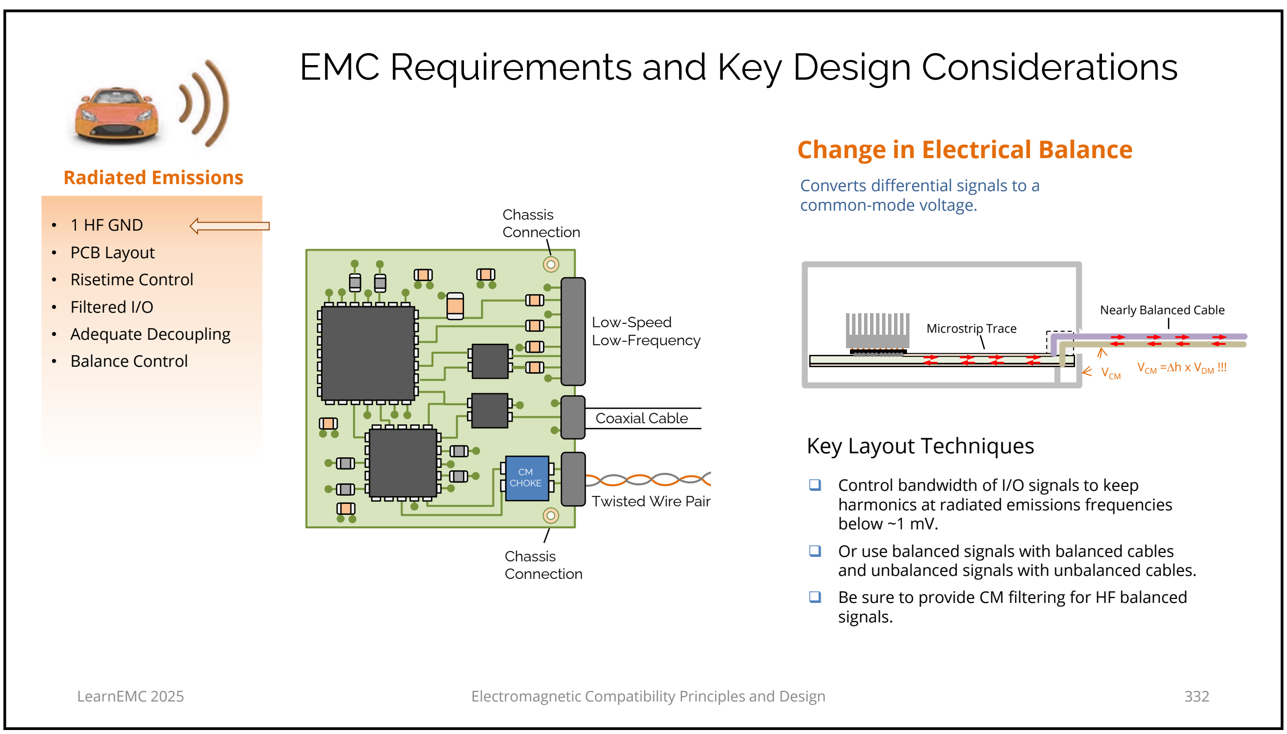
EMC Requirements and Key Design Considerations
Radiated Emissions
• 1 HF GND
• PCB Layout
• Risetime Control
• Filtered I/O
• Adequate Decoupling
• Balance Control
Chassis Connection
Low-Speed Low-Frequency
Coaxial Cable
CM CHOKE
Twisted Wire Pair
Chassis Connection
Change in Electrical Balance
Converts differential signals to a common-mode voltage.
Nearly Balanced Cable
Microstrip Trace
VCM
VCM =Δh x VDM !!!
Key Layout Techniques
❑ Control bandwidth of I/O signals to keep harmonics at radiated emissions frequencies below ~1 mV.
❑ Or use balanced signals with balanced cables and unbalanced signals with unbalanced cables.
❑ Be sure to provide CM filtering for HF balanced signals.
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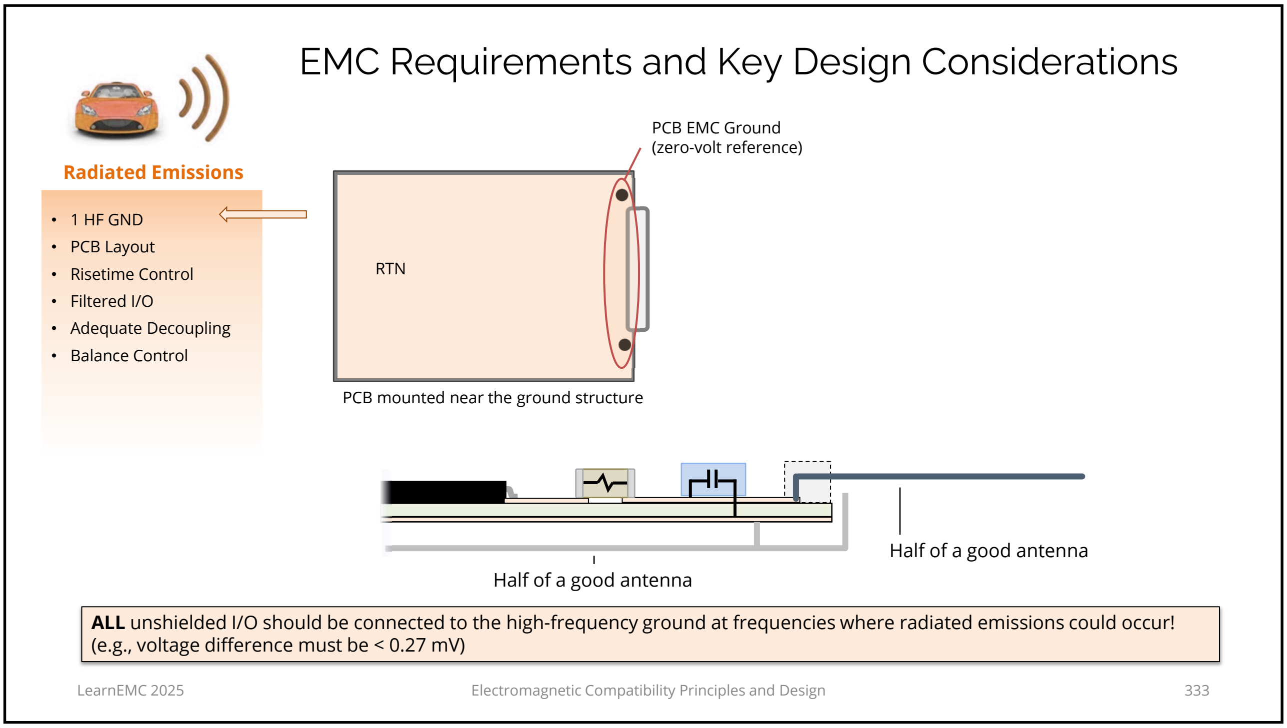
EMC Requirements and Key Design Considerations
Radiated Emissions
• 1 HF GND
• PCB Layout
• Risetime Control
• Filtered I/O
• Adequate Decoupling
• Balance Control
PCB EMC Ground
(zero-volt reference)
RTN
PCB mounted near the ground structure
Half of a good antenna
Half of a good antenna
ALL unshielded I/O should be connected to the high-frequency ground at frequencies where radiated emissions could occur!
(e.g., voltage difference must be < 0.27 mV)
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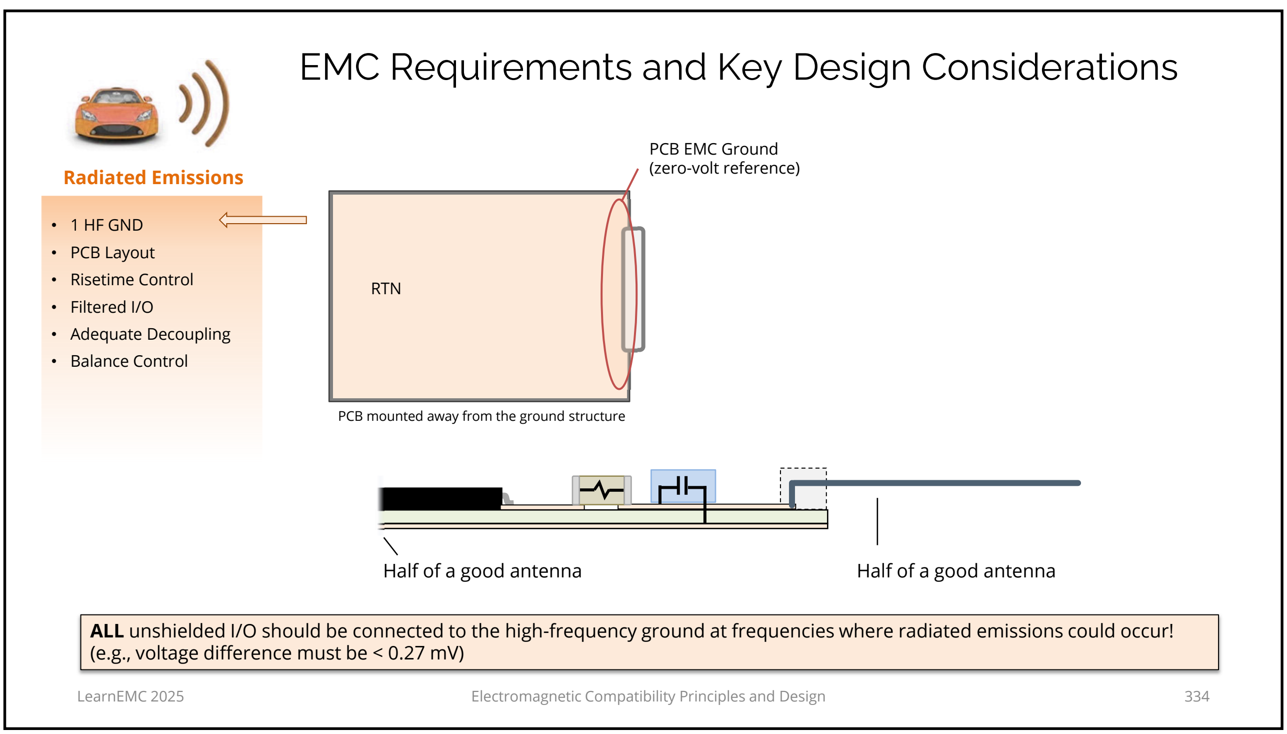
EMC Requirements and Key Design Considerations
Radiated Emissions
• 1 HF GND
• PCB Layout
• Risetime Control
• Filtered I/O
• Adequate Decoupling
• Balance Control
PCB EMC Ground
(zero-volt reference)
RTN
PCB mounted away from the ground structure
Half of a good antenna
Half of a good antenna
ALL unshielded I/O should be connected to the high-frequency ground at frequencies where radiated emissions could occur!
(e.g., voltage difference must be < 0.27 mV)
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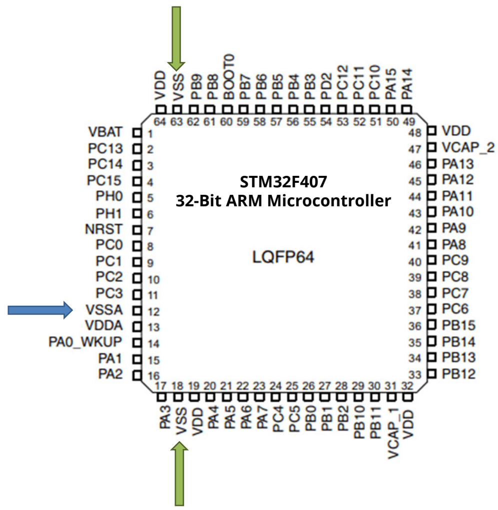
Radiated Emissions

- 1 HF GND
- PCB Layout
- Risetime Control
- Filtered I/O
- Adequate Decoupling
- Balance Control

EMC Requirements and Key Design Considerations



Don't isolate returns!

No matter what the datasheet says!

Unless you've been able to prove that it is necessary.

$$V_{coupled} = I_{source} \times R_{shared}$$

(worst-case) (worst-case) (worst-case)

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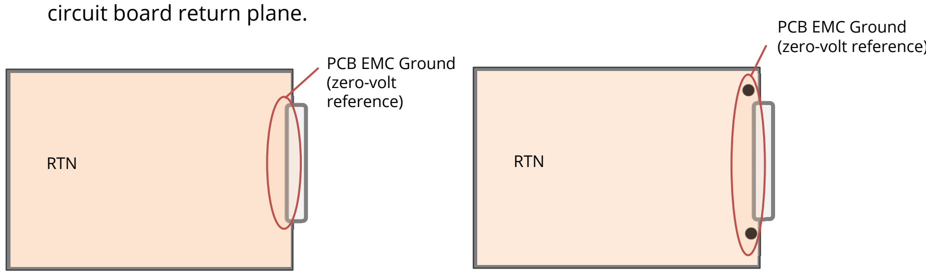
Radiated Emissions

- 1 HF GND
- PCB Layout
- Risetime Control
- Filtered I/O
- Adequate Decoupling
- Balance Control

EMC Requirements and Key Design Considerations

Connecting Cable Shields on the PCB

- ❑ Cable shields should ALWAYS connect directly to the chassis.
- ❑ If they must connect to the board first, it must be to the PCB EMC Ground.
- ❑ If the cable shield returns intentional current, it must ALSO connect to the circuit board return plane.



PCB in product with no ground structure

PCB mounted near the ground structure

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EMC Requirements and Key Design Considerations

Radiated Emissions

- 1 HF GND
- PCB Layout
- Risetime Control
- Filtered I/O
- Adequate Decoupling
- Balance Control

What about frequencies above a few hundred MHz?

- Cables are much less likely to be the antenna.
- Most common GHz antenna on a PCB is lightly loaded planes.
  - Ground planes should be stitched together frequently.
  - Power planes should be close to ground planes (e.g., < 0.25 mm)
  - Power planes should have lots of connections (active devices and decoupling capacitors)
  - Don't extend power planes to areas of the board where they are not used, and don't allow one section of power plane to become choked off from another section.
  - Avoid having large-valued ceramic capacitors connected to the same power/ground plane pairs as high-valued ceramic capacitors. They will support a parasitic oscillation typically at GHz frequencies.
- Most common GHz antenna in a system is enclosure seams or slots backed by a resonant enclosure cavity.

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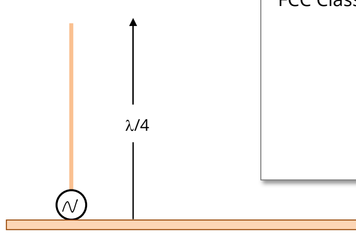
EMC Requirements and Key Design Considerations

Radiated Emissions

- 1 HF GND
- PCB Layout
- Risetime Control
- Filtered I/O
- Adequate Decoupling
- Balance Control



Average radiated power required to exceed FCC Class B Limit:

$$P_{rad} = \frac{|E|^2}{\eta}\frac{2\pi r^2}{D_0} = \frac{|100\,\mu V/m|^2}{377\,\Omega}\frac{2\pi(3\,m)^2}{1.6} \approx 1\,nW$$

Voltage driving a resonant monopole required to exceed FCC Class B Limit:

$$V = \sqrt{P_{rad}R_{rad}} = \sqrt{(1\,nW)(36\,\Omega)} \approx 0.19\,mV$$

$I_{max} = 5.3\ \mu A$

If the voltage between any two large metallic structures is on the order of a millivolt at 30 MHz or higher, there is usually cause for concern.

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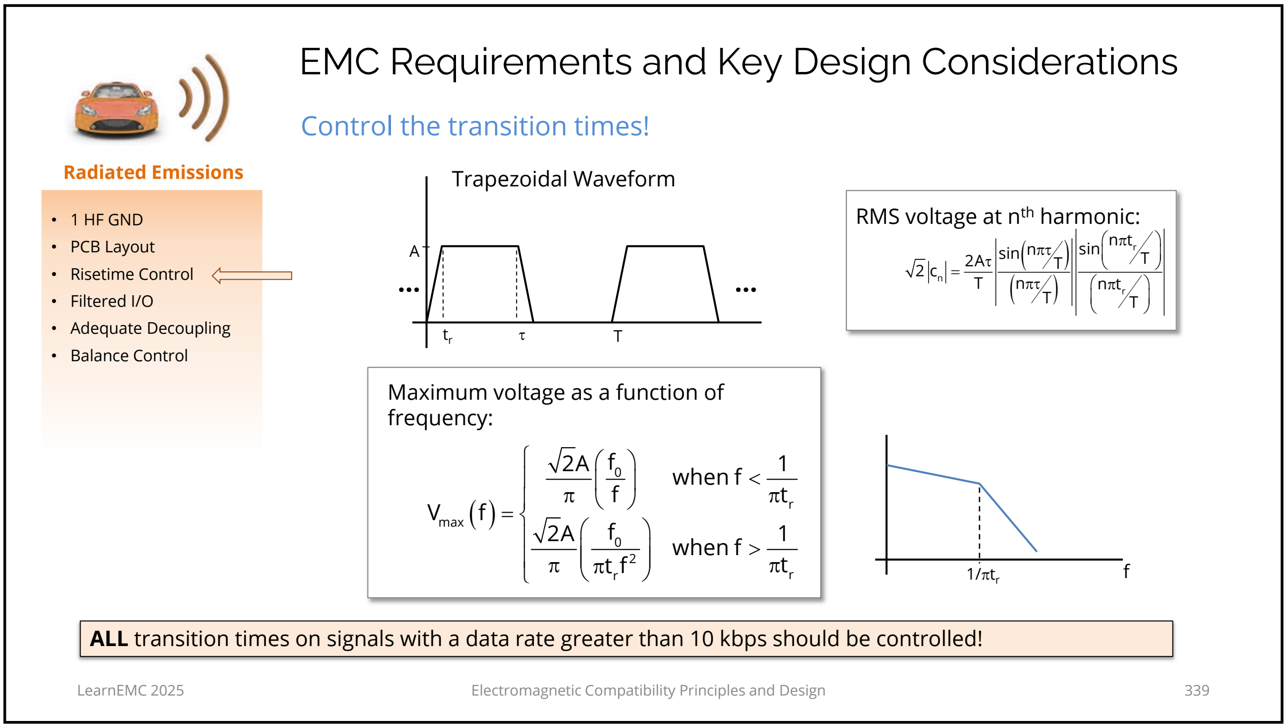
EMC Requirements and Key Design Considerations
Control the transition times!
Radiated Emissions
1 HF GND
PCB Layout
Risetime Control
Filtered I/O
Adequate Decoupling
Balance Control
Trapezoidal Waveform
A
t_r
τ
T
RMS voltage at n^{th} harmonic:
$\sqrt{2}|c_n| = \frac{2A\tau}{T}\left|\frac{\sin\left(\frac{n\pi\tau}{T}\right)}{\left(\frac{n\pi\tau}{T}\right)}\right|\left|\frac{\sin\left(\frac{n\pi t_r}{T}\right)}{\left(\frac{n\pi t_r}{T}\right)}\right|$
Maximum voltage as a function of frequency:
$V_{max}(f) = \begin{cases} \frac{\sqrt{2}A}{\pi}\left(\frac{f_0}{f}\right) & \text{when } f < \frac{1}{\pi t_r} \\ \frac{\sqrt{2}A}{\pi}\left(\frac{f_0}{\pi t_r f^2}\right) & \text{when } f > \frac{1}{\pi t_r} \end{cases}$
$1/\pi t_r$
f
ALL transition times on signals with a data rate greater than 10 kbps should be controlled!
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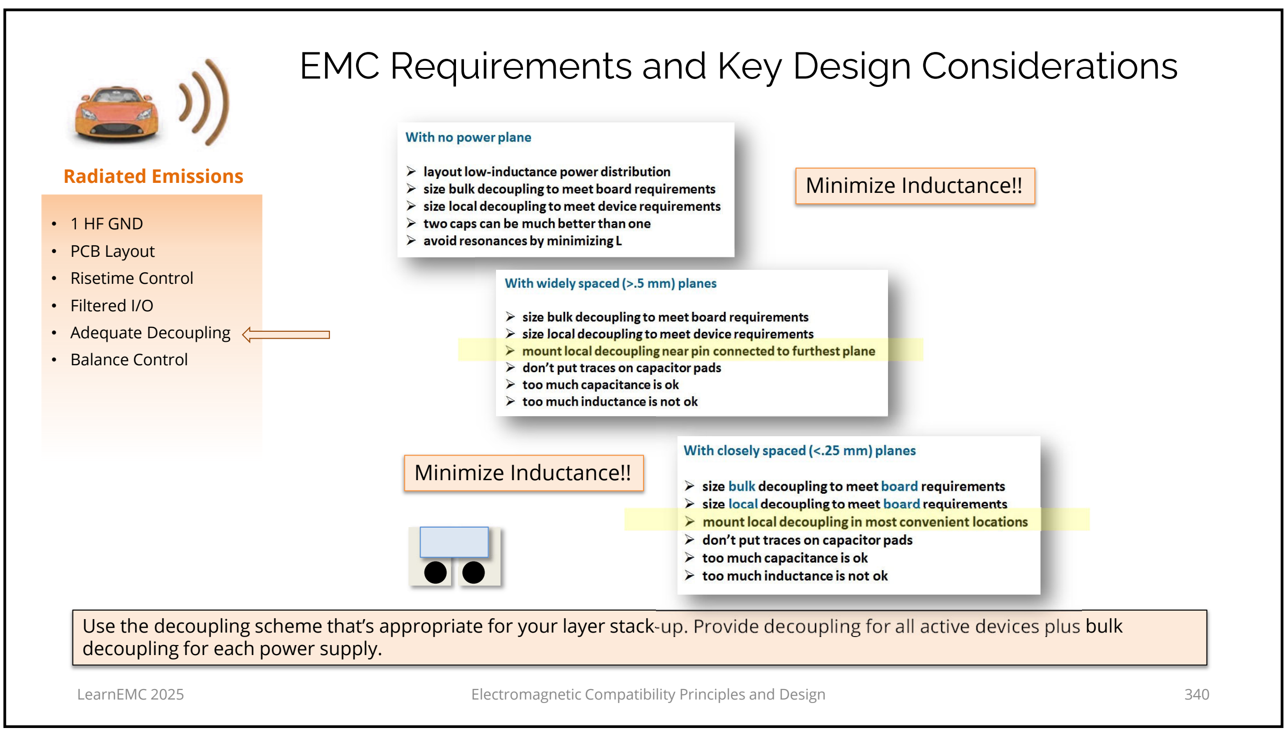
EMC Requirements and Key Design Considerations
Radiated Emissions
1 HF GND
PCB Layout
Risetime Control
Filtered I/O
Adequate Decoupling
Balance Control
With no power plane
layout low-inductance power distribution
size bulk decoupling to meet board requirements
size local decoupling to meet device requirements
two caps can be much better than one
avoid resonances by minimizing L
Minimize Inductance!!
With widely spaced (>.5 mm) planes
size bulk decoupling to meet board requirements
size local decoupling to meet device requirements
mount local decoupling near pin connected to furthest plane
don't put traces on capacitor pads
too much capacitance is ok
too much inductance is not ok
Minimize Inductance!!
With closely spaced (<.25 mm) planes
size bulk decoupling to meet board requirements
size local decoupling to meet board requirements
mount local decoupling in most convenient locations
don't put traces on capacitor pads
too much capacitance is ok
too much inductance is not ok
Use the decoupling scheme that's appropriate for your layer stack-up. Provide decoupling for all active devices plus bulk decoupling for each power supply.
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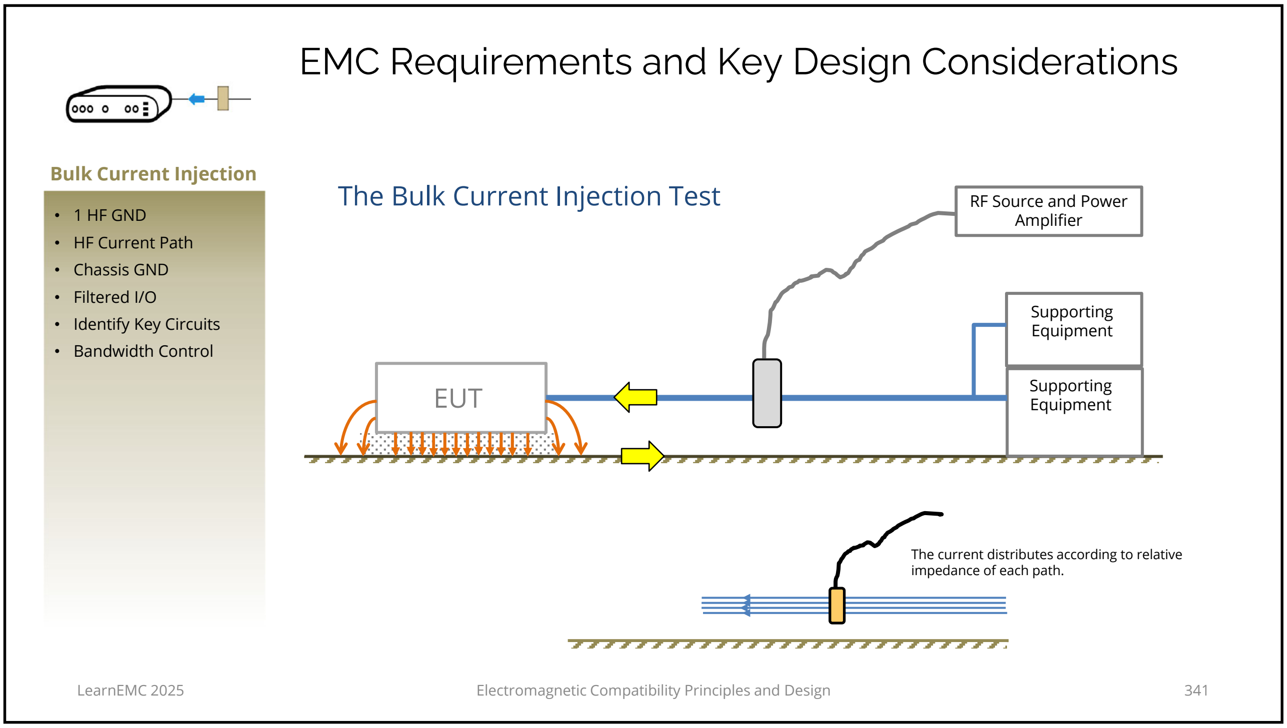
EMC Requirements and Key Design Considerations
Bulk Current Injection
1 HF GND
HF Current Path
Chassis GND
Filtered I/O
Identify Key Circuits
Bandwidth Control
The Bulk Current Injection Test
RF Source and Power Amplifier
Supporting Equipment
Supporting Equipment
EUT
The current distributes according to relative impedance of each path.
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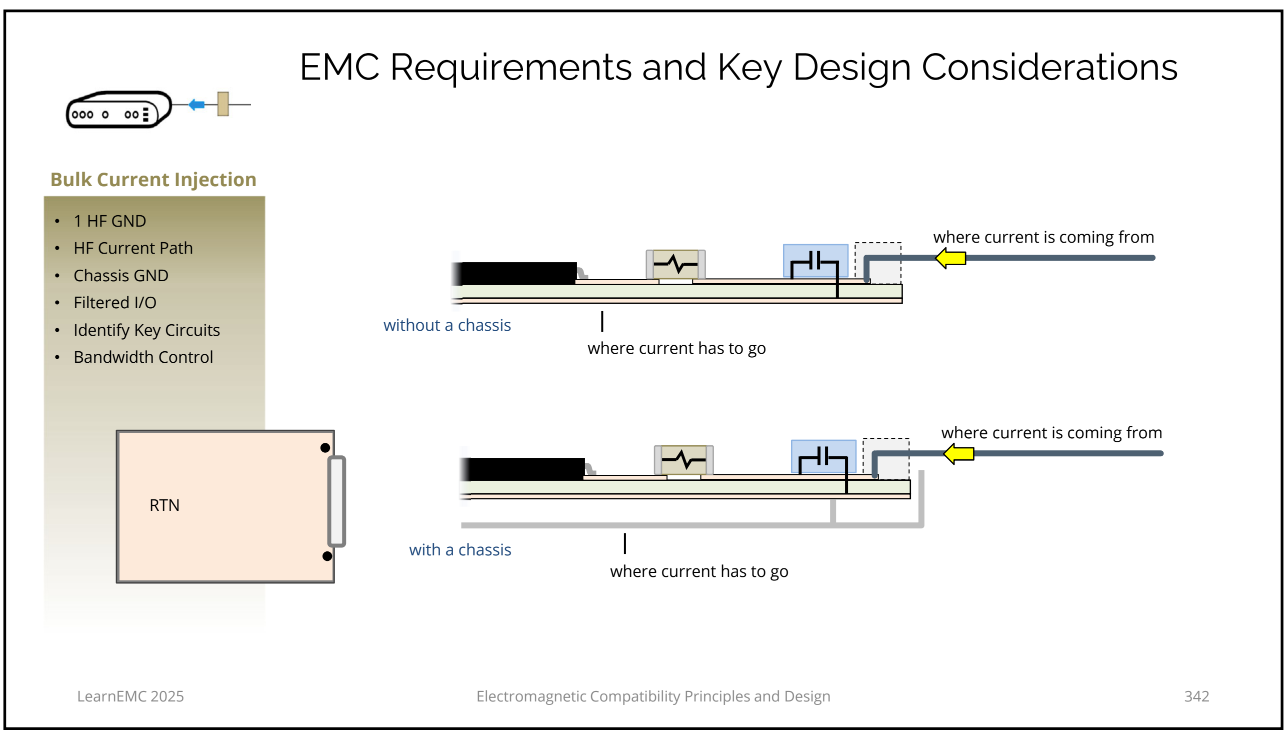
EMC Requirements and Key Design Considerations
Bulk Current Injection
1 HF GND
HF Current Path
Chassis GND
Filtered I/O
Identify Key Circuits
Bandwidth Control
RTN
where current is coming from
without a chassis
where current has to go
where current is coming from
with a chassis
where current has to go
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Electromagnetic Compatibility Principles and Design
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EMC Requirements and Key Design Considerations

Radiated Immunity

- 1 HF GND
- Filtered I/O
- Transition Times
- Victim Identification
- Adequate Decoupling
- Balance Control

1. First do the BCI evaluation
2. Also look for direct field coupling
3. Identify potential victim circuits
4. Identify the coupling path(s)
   - Electric field coupled
   - Magnetic field coupled
5. Calculate the worst-case coupling to each victim circuit

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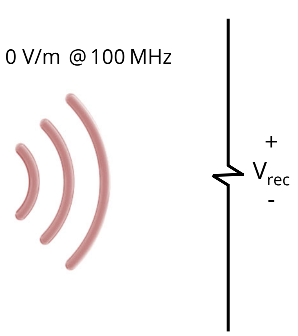
EMC Requirements and Key Design Considerations

Radiated Immunity

- 1 HF GND
- Filtered I/O
- Transition Times
- Victim Identification
- Adequate Decoupling
- Balance Control

Electric Field Coupling

$\left|\vec{E}_{inc}\right| = 10\ \text{V/m}\ @\ 100\ \text{MHz}$



For matched resonant dipole:

$$\mathcal{P}_{rec} = \frac{\left|10\ \text{V/m}\right|^2}{377\ \Omega} = 0.26\ \text{W/m}^2$$

$$A_e = \frac{(3)^2}{4\pi}1.64 = 1.17\ \text{m}^2$$

$$P_{rec} = \left(0.26\ \text{W/m}^2\right)\left(1.17\ \text{m}^2\right)(1) = 0.30\ \text{W}$$

$$V_{rec} = \sqrt{RP_{rec}} = \sqrt{(72\ \Omega)(0.30\ \text{W})} = 4.7\ \text{V}$$

Note: The open-circuit voltage would be approximately twice this value or 10 volts.

Useful Approximate Solution:

$$V_{rec-max} \approx L_{antenna} E_{inc}$$

$$V_{rec-max} \approx 1.5\ \text{m}(10\ \text{V/m}) = 15\ \text{V}$$

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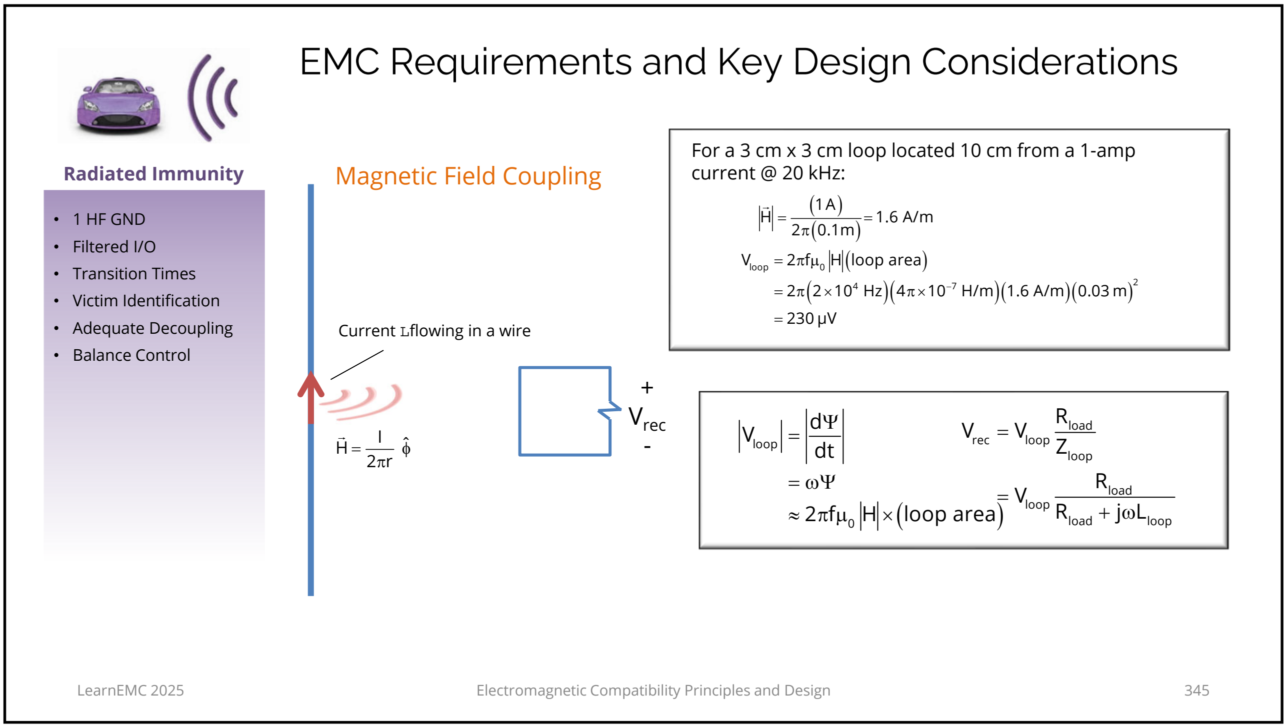
EMC Requirements and Key Design Considerations
Radiated Immunity
• 1 HF GND
• Filtered I/O
• Transition Times
• Victim Identification
• Adequate Decoupling
• Balance Control
Magnetic Field Coupling
Current I flowing in a wire
$\vec{H} = \frac{I}{2\pi r}\hat{\phi}$
+
V_{rec}
-
For a 3 cm x 3 cm loop located 10 cm from a 1-amp current @ 20 kHz:
$|\vec{H}| = \frac{(1\,A)}{2\pi(0.1\,m)} = 1.6\ A/m$
$V_{loop} = 2\pi f\mu_0 |H|(\text{loop area})$
$= 2\pi(2\times10^4\ Hz)(4\pi\times10^{-7}\ H/m)(1.6\ A/m)(0.03\ m)^2$
$= 230\ \mu V$
$|V_{loop}| = \left|\frac{d\Psi}{dt}\right| = \omega\Psi \approx 2\pi f\mu_0 |H| \times (\text{loop area})$
$V_{rec} = V_{loop}\frac{R_{load}}{Z_{loop}} = V_{loop}\frac{R_{load}}{R_{load} + j\omega L_{loop}}$
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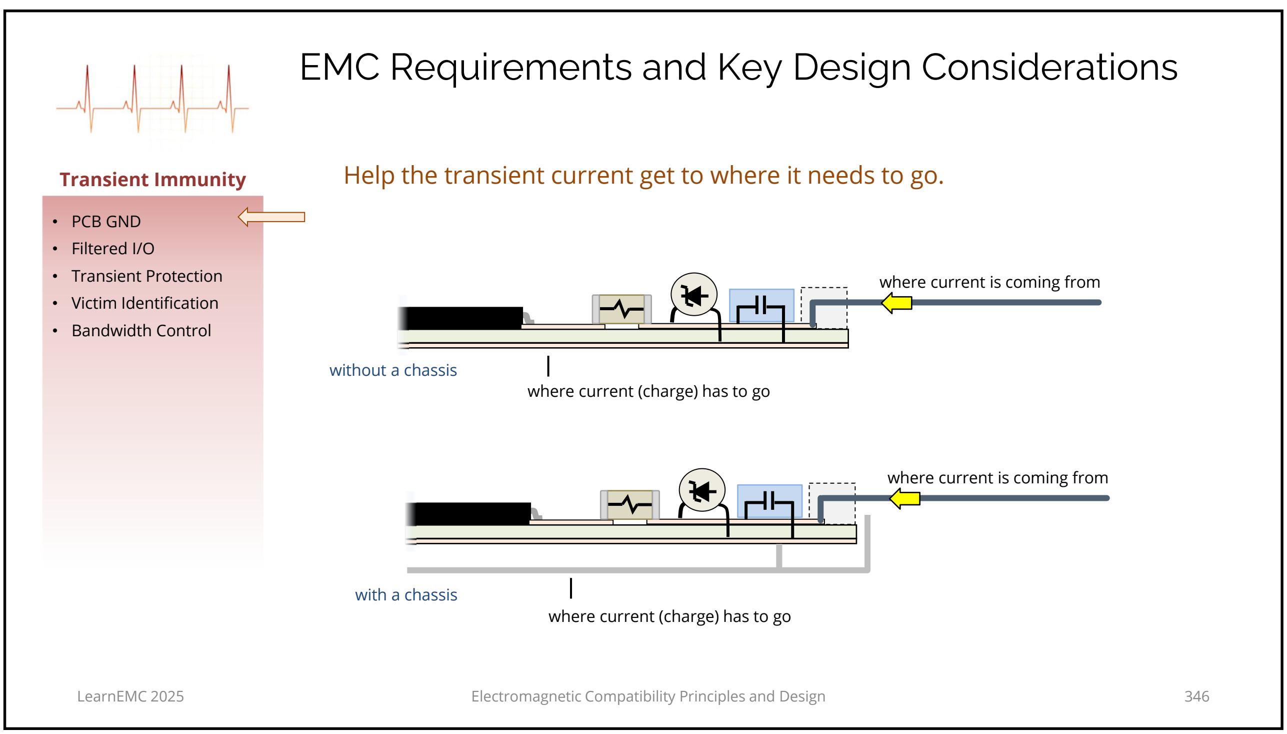
EMC Requirements and Key Design Considerations
Transient Immunity
• PCB GND
• Filtered I/O
• Transient Protection
• Victim Identification
• Bandwidth Control
Help the transient current get to where it needs to go.
where current is coming from
without a chassis
where current (charge) has to go
where current is coming from
with a chassis
where current (charge) has to go
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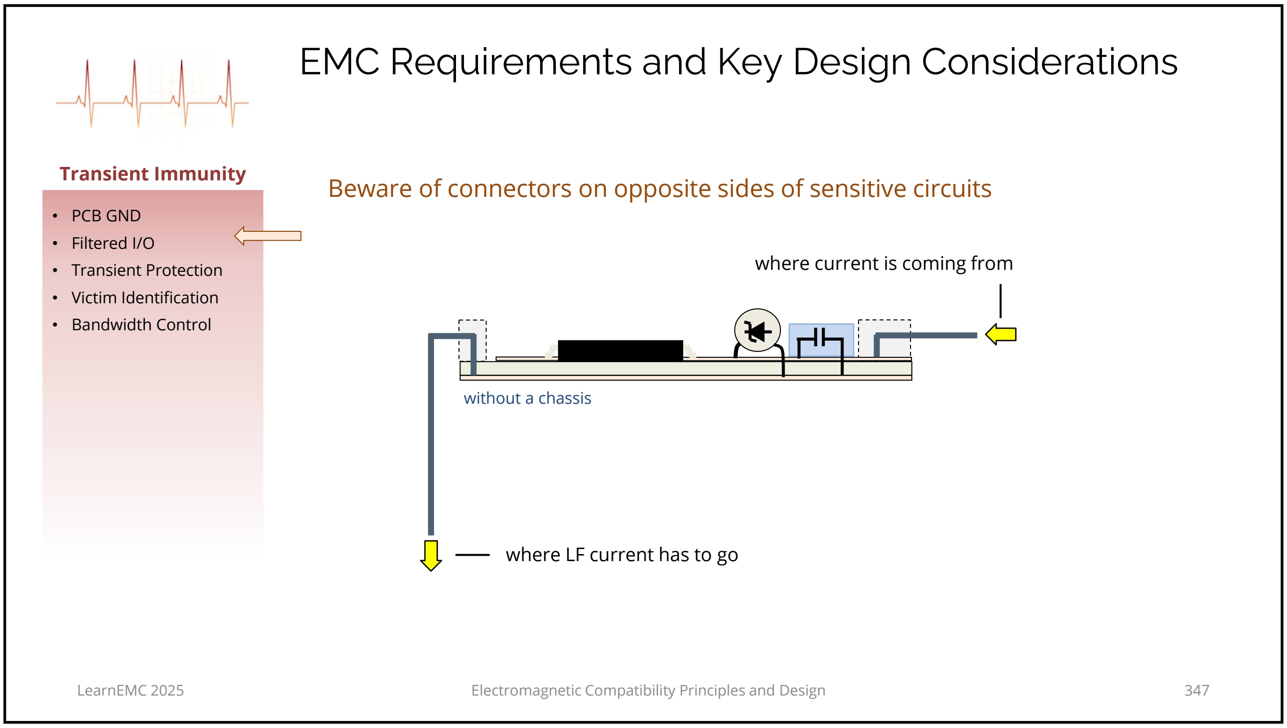
Electromagnetic Compatibility Principles and Design
346


EMC Requirements and Key Design Considerations
Transient Immunity
PCB GND
Filtered I/O
Transient Protection
Victim Identification
Bandwidth Control
Beware of connectors on opposite sides of sensitive circuits
where current is coming from
without a chassis
where LF current has to go
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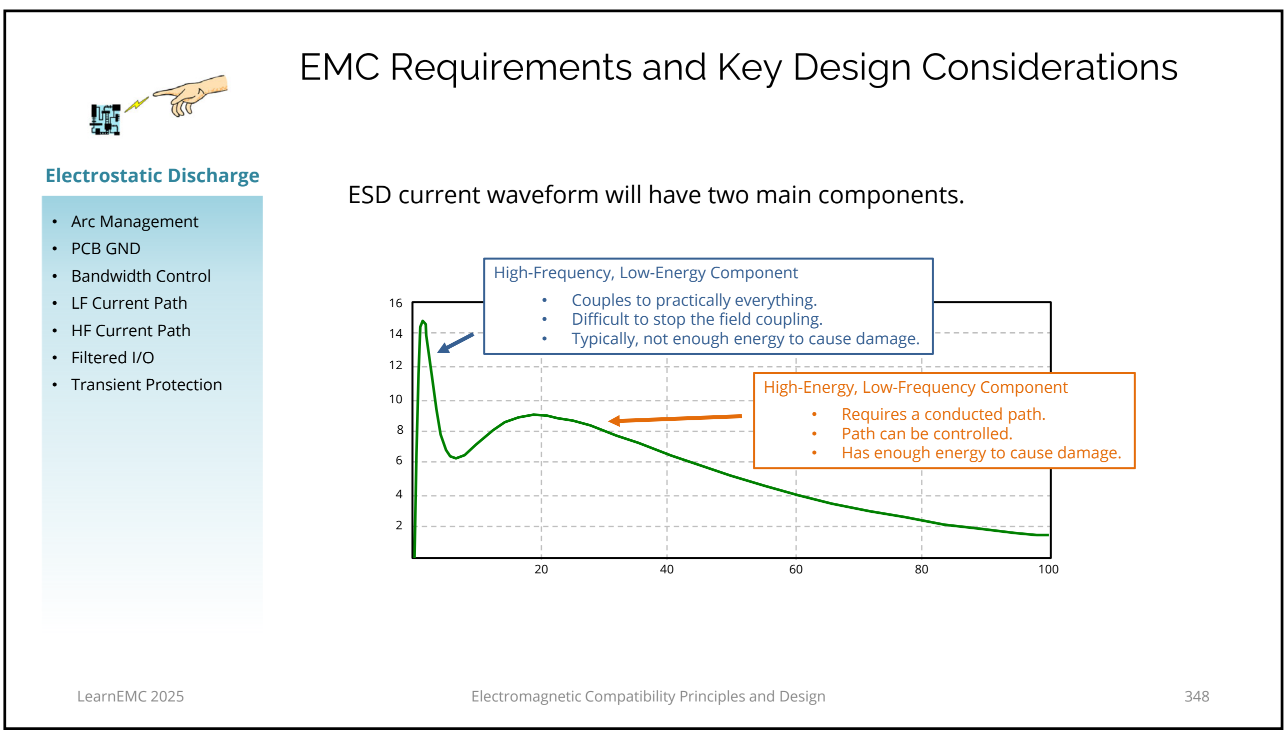
EMC Requirements and Key Design Considerations
Electrostatic Discharge
Arc Management
PCB GND
Bandwidth Control
LF Current Path
HF Current Path
Filtered I/O
Transient Protection
ESD current waveform will have two main components.
High-Frequency, Low-Energy Component
Couples to practically everything.
Difficult to stop the field coupling.
Typically, not enough energy to cause damage.
High-Energy, Low-Frequency Component
Requires a conducted path.
Path can be controlled.
Has enough energy to cause damage.
16
14
12
10
8
6
4
2
20
40
60
80
100
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Electromagnetic Compatibility Principles and Design
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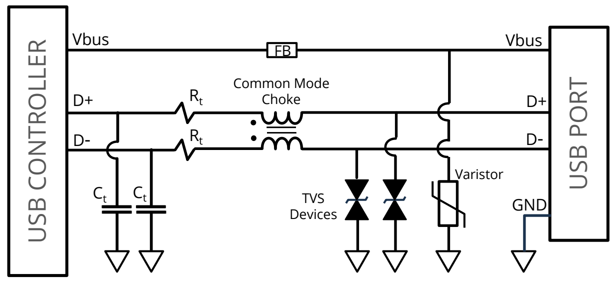
EMC Requirements and Key Design Considerations

Electrostatic Discharge

- Arc Management
- PCB GND
- Bandwidth Control
- LF Current Path
- HF Current Path
- Filtered I/O
- Transient Protection

High-Energy, Low-Frequency Component
- Requires a conducted path.
- Path can be controlled.
- Has enough energy to cause damage.



There are customized ESD protection circuits for standard interfaces such as USB, SCSI and HDMI.

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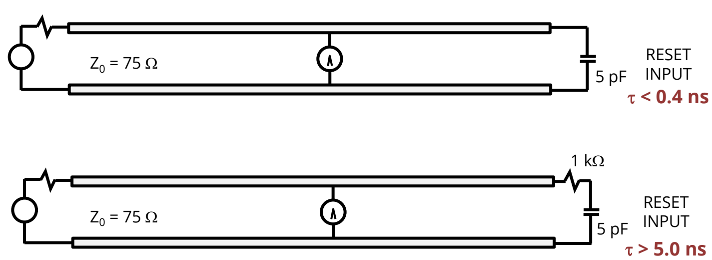
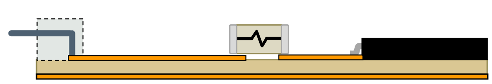
EMC Requirements and Key Design Considerations

Electrostatic Discharge

- Arc Management
- PCB GND
- Bandwidth Control
- LF Current Path
- HF Current Path
- Filtered I/O
- Transient Protection

High-Frequency, Low-Energy Component
- Couples to practically everything.
- Difficult to stop the field coupling.
- Typically, not enough energy to cause damage.





Put a resistor in series with IC inputs and outputs.

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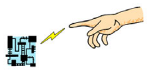
EMC Requirements and Key Design Considerations



Electrostatic Discharge

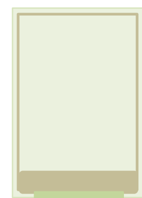
- Arc Management
- PCB GND
- Bandwidth Control
- LF Current Path
- HF Current Path
- Filtered I/O
- Transient Protection

ESD Entry Points

- ❑ Seams
- ❑ Touch Panels
- ❑ Connector Pins

What is an ESD ground?

An ESD ground is a conductor placed in a position to intercept an electrostatic discharge and route the current harmlessly to its destination. This is often a ring of ground around the outside of a board between the enclosure seams and the rest of the circuitry. ESD grounds only make a connection to system ground at a single point.



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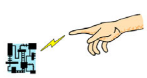
EMC Requirements and Key Design Considerations



Electrostatic Discharge

- Arc Management
- PCB GND
- Bandwidth Control
- LF Current Path
- HF Current Path
- Filtered I/O
- Transient Protection

High-Frequency, Low-Energy Component
- Couples to practically everything.
- Difficult to stop the field coupling.
- Typically, not enough energy to cause damage.

High-Energy, Low-Frequency Component
- Requires a conducted path.
- Path can be controlled.
- Has enough energy to cause damage.

- ✓✓ ❑ Prevent the discharge from occurring
- ✓ ❑ Control the flow of low-frequency currents with transient protection
- ✓ ❑ Control the flow of high-frequency currents with routing
- ✓ ❑ Watch for arc-paths
- ✓✓ ❑ Watch for E-field and H-field coupling
- ✓✓ ❑ Series resistance slows transition times, reduces field coupling
- ✓ ❑ TVS diodes or varistors protect sensitive IC inputs from damage

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Electromagnetic Compatibility Principles and Design
An EMC Compliance Strategy
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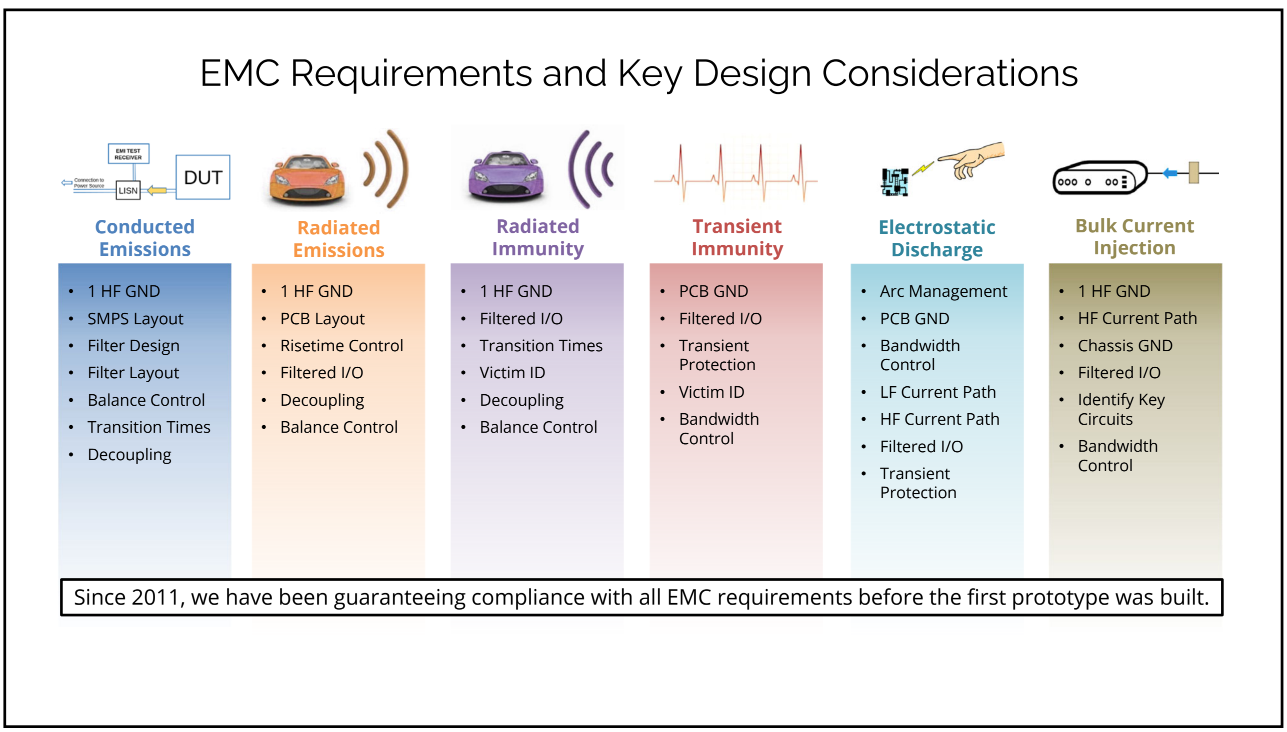
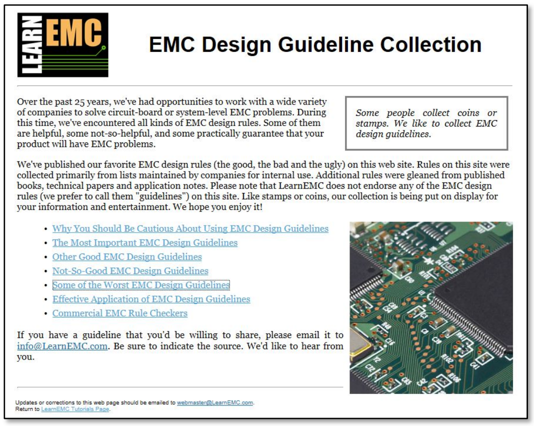

EMC Requirements and Key Design Considerations
EMI TEST RECEIVER
DUT
LISN
Conducted Emissions
1 HF GND
SMPS Layout
Filter Design
Filter Layout
Balance Control
Transition Times
Decoupling
Radiated Emissions
1 HF GND
PCB Layout
Risetime Control
Filtered I/O
Decoupling
Balance Control
Radiated Immunity
1 HF GND
Filtered I/O
Transition Times
Victim ID
Decoupling
Balance Control
Transient Immunity
PCB GND
Filtered I/O
Transient Protection
Victim ID
Bandwidth Control
Electrostatic Discharge
Arc Management
PCB GND
Bandwidth Control
LF Current Path
HF Current Path
Filtered I/O
Transient Protection
Bulk Current Injection
1 HF GND
HF Current Path
Chassis GND
Filtered I/O
Identify Key Circuits
Bandwidth Control
Since 2011, we have been guaranteeing compliance with all EMC requirements before the first prototype was built.

What we are NOT doing



EMC Design Guideline Collection

Over the past 25 years, we've had opportunities to work with a wide variety of companies to solve circuit-board or system-level EMC problems. During this time, we've encountered all kinds of EMC design rules. Some of them are helpful, some not-so-helpful, and some practically guarantee that your product will have EMC problems.

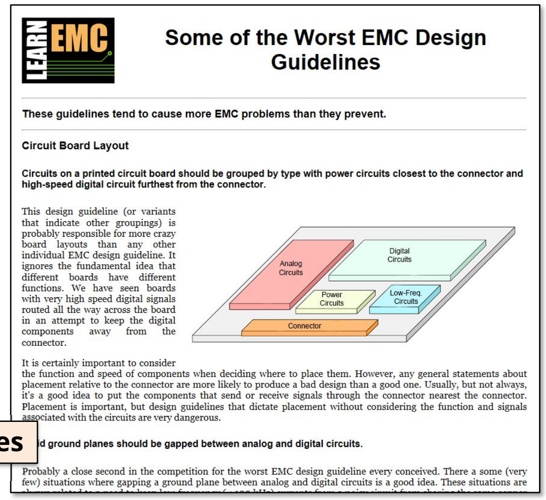
Some people collect coins or stamps. We like to collect EMC design guidelines.

We've published our favorite EMC design rules (the good, the bad and the ugly) on this web site. Rules on this site were collected primarily from lists maintained by companies for internal use. Additional rules were gleaned from published books, technical papers and application notes. Please note that LearnEMC does not endorse any of the EMC design rules (we prefer to call them "guidelines") on this site. Like stamps or coins, our collection is being put on display for your information and entertainment. We hope you enjoy it!

- Why You Should Be Cautious About Using EMC Design Guidelines
- The Most Important EMC Design Guidelines
- Other Good EMC Design Guidelines
- Not-So-Good EMC Design Guidelines
- Some of the Worst EMC Design Guidelines
- Effective Application of EMC Design Guidelines
- Commercial EMC Rule Checkers

If you have a guideline that you'd be willing to share, please email it to info@LearnEMC.com. Be sure to indicate the source. We'd like to hear from you.

Updates or corrections to this web page should be emailed to webmaster@LearnEMC.com.
Return to LearnEMC Tutorials Page.



Some of the Worst EMC Design Guidelines

These guidelines tend to cause more EMC problems than they prevent.

Circuit Board Layout

Circuits on a printed circuit board should be grouped by type with power circuits closest to the connector and high-speed digital circuit furthest from the connector.

This design guideline (or variants that indicate other groupings) is probably responsible for more crazy board layouts than any other individual EMC design guideline. It ignores the fundamental idea that different boards have different functions. We have seen boards with very high speed digital signals routed all the way across the board in an attempt to keep the digital components away from the connector.

It is certainly important to consider the function and speed of components when deciding where to place them. However, any general statements about placement relative to the connector are more likely to produce a bad design than a good one. Usually, but not always, it's a good idea to put the components that send or receive signals through the connector nearest the connector. Placement is important, but design guidelines that dictate placement without considering the function and signals associated with the circuits are very dangerous.

...id ground planes should be gapped between analog and digital circuits.

Probably a close second in the competition for the worst EMC design guideline every conceived. There a some (very few) situations where gapping a ground plane between analog and digital circuits is a good idea. These situations are

<u>NOT</u> Relying on EMC Design Guidelines

What we are NOT doing

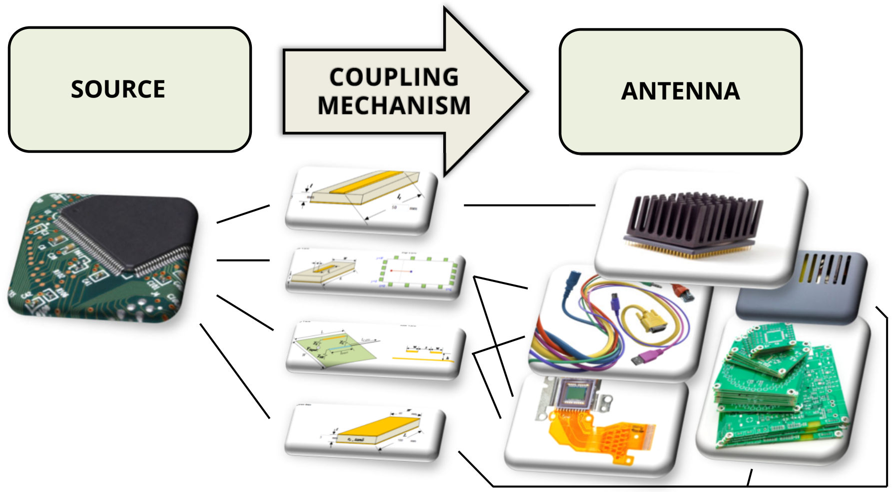
Numerical EM modeling codes give precise answers to precisely defined problems. EMC geometries are not well-defined.

We don't want to know how much a given configuration will radiate. The answer to that question depends on a lot of factors that we have no control over.

We want to know our product will meet its requirements.

<u>NOT</u> Modeling Products with Numerical EM Modeling Codes

What we ARE doing



Identifying all possible sources, victims and coupling paths

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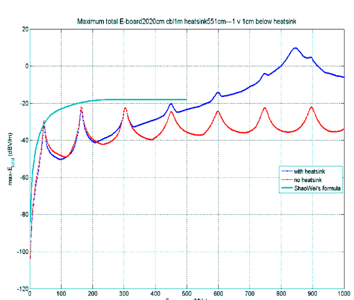
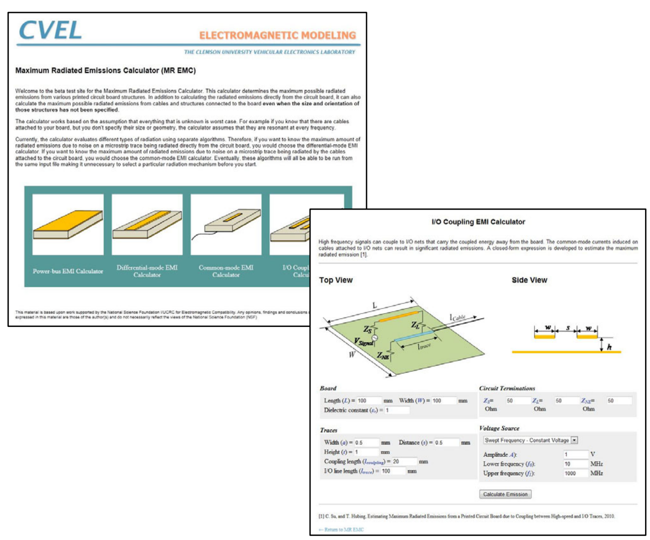
Maximum Radiated Emissions Concept





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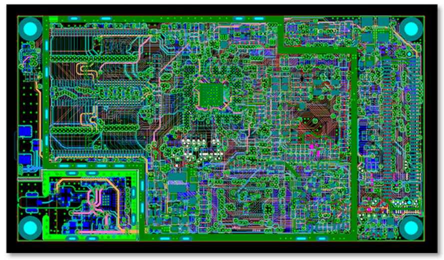
Things Required for the PCB EMC Design Review

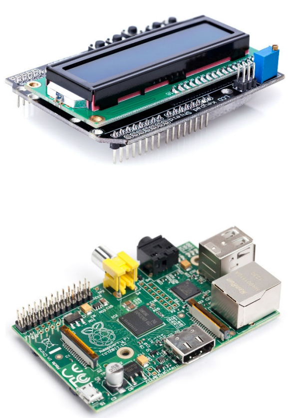


- Board layout files
- Schematics
- General familiarity with system design and function
- General familiarity with system EMC requirements
- Access to board/circuit designers

Sample PCB Layout Design Review Steps

1. Identify connections to ground structure and locations of all I/O.
2. Identify ground plane layer(s) and extent of plane.
   - Should be solid (not gapped).
   - If gapped, nothing should cross over the gap.
   - If missing in an area, all currents in that area should be traced and all nets scrutinized.
3. Identify ground traces/fills on other layers.
   - There should be no ground traces except where absolutely necessary to isolate current returns.
   - Any component gnd pin connecting to gnd fill should have a via to gnd plane at the pin.
4. Identify power distribution layer(s) and type of power distribution (WSP/CSP/NP).
   - Generally, no two power fills should overlap.
   - Power should only be routed where it is required.
   - Power return currents should flow next to power delivery currents.
   - Identify location and values of all decoupling capacitors for each power net
   - Identify mounting structure details for all decoupling capacitors to ensure they are appropriate.
5. Identify I/O nets.
   - Capacitor to HF ground and/or series resistance, CM isolation, or shielded connector
   - Appropriate transient protection
   - Terminated near connector with no opportunity for crosstalk from other circuits.
6. Identify filter components.
   - Establish a quiet side and a noisy side.
   - Look for parasitic coupling paths that might allow HF noise to bypass the filter.

Sample PCB Layout Design Review Steps



7. Identify traces requiring transition-time control with series resistance.
   - All traces connected to devices with internally generated clocks
   - Long traces
   - Traces connected to reset or other critical inputs
   - Traces that don't have a solid return plane on an adjacent layer for their entire length
   - Traces that run near the edge of the return plane
   - Traces that run near other traces carrying much stronger or much weaker signals
8. Identify critical components.
   - Orient inductors to reduce coupling from their external magnetic fields.
   - Examine op amp circuits to minimize electric and magnetic field coupling.
   - Ensure transient protection components connect to the proper "ground."
   - PLLs – filter power, but not ground.
   - Ferrites – ensure proper frequency range and saturation current. (use resistor instead?)
   - Ferrites – no ferrite should be connected to any net labeled "gnd."
9. Identify power inverter circuits/devices.
   - Minimize area of switching nodes.
   - Minimize loop area of switching currents and keep them off ground plane if necessary.
   - Look for unintended coupling from magnetics.
10. Identify EMC test ports.
   - Move HF circuitry that is between connectors (or shield the enclosure).
   - Trace BCI currents from injection points to chassis ground (should not come onto board).
   - Trace EFT currents from injection points to chassis ground, watch for unwanted coupling.
   - Trace LF ESD currents from injection points to chassis ground.
   - Trace HF ESD currents from injection points to "big metal."

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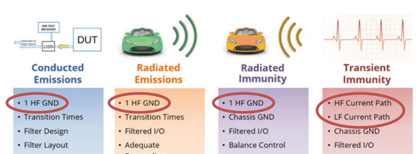
System Design: Identify and Utilize the Ground Structure!



- Don't try to isolate low-voltage power returns from the chassis!
- Components with a wire harness that are mounted near the chassis should make a good HF connection to the chassis.
- DC isolation is a last-resort. Only do this when a clear common-impedance coupling problem has been documented and better methods of dealing with the issue are unavailable.
- Ensure that all large metal structures are electrically well-connected.

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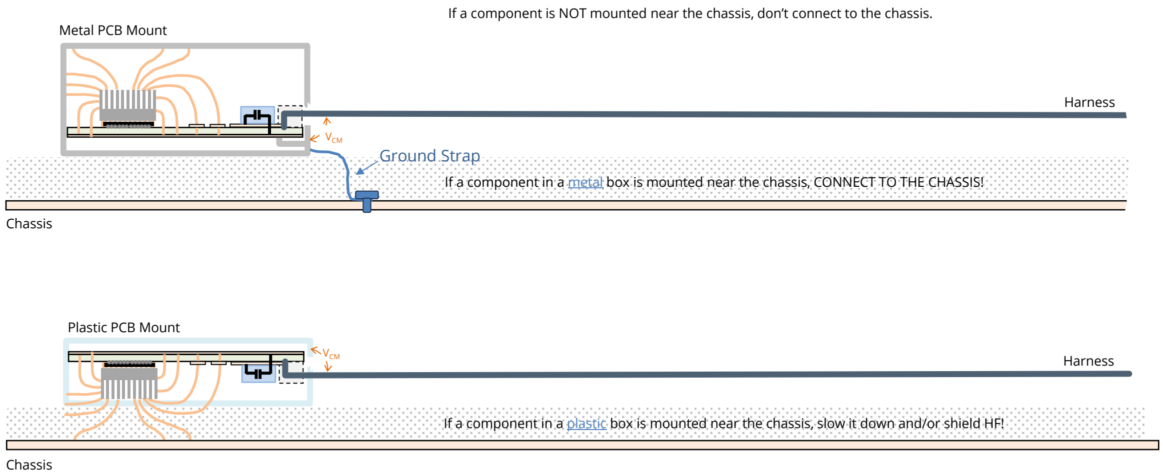
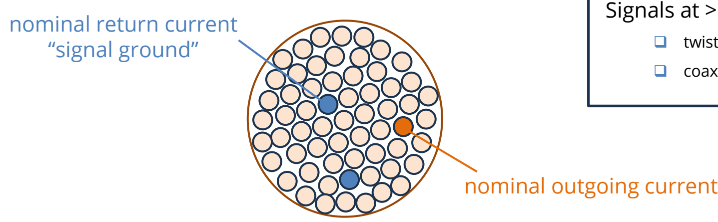
System Design: Component Mounting



System Design: Harness Layout

Where does the 10 MHz return current flow?

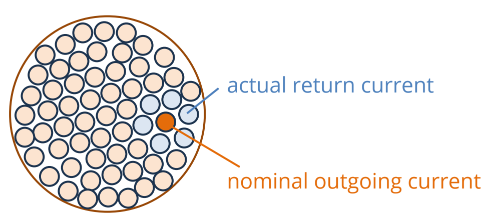


Signals at > 1 Mbps in a harness must use:

- twisted-wire pair with a CM choke (differential signals)
- coaxial cable (single-ended signals).

In a vehicle wiring harness:

- intentional >1 MHz signals are differential
- all other signals wires are band-limited.



Expect crosstalk between signals in a harness!

Don't wait to see if there is a problem before doing this!
Harness crosstalk problems tend to show up at inconvenient times!

At high-frequencies (e.g., 100 kHz and higher)

Expect -20 dB of coupling between any circuits sharing any part of a wiring harness!
(Unless you've explicitly calculated the worst-case coupling.)

At low-frequencies (e.g., below 100 kHz)

Do a worst-case calculation of common-impedance coupling between any two circuits sharing a wiring harness!

$$V_{\text{coupled (worst-case)}} = I_{\text{source (worst-case)}} \times R_{\text{shared (worst-case)}}$$

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Summary of Design Strategy

- Control all transitions times and signal bandwidths. This will help you identify and define your sources as well as potential coupling paths and antennas.
- Identify all potential antennas for radiated emissions/immunity and ports for conducted emissions/immunity.
- Trace low-frequency currents (signals and applied noise) while looking for potential common-impedance coupling to sensitive circuits.
- Trace high-frequency currents looking for voltage drops that might facilitate coupling between antenna halves.
- Employ filtering and transient protection as needed to keep worst-case coupling below levels that could cause system to fail to meet EMC requirements.

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Design Strategies and Examples

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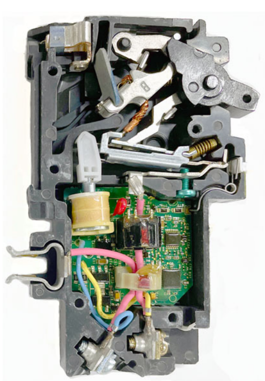
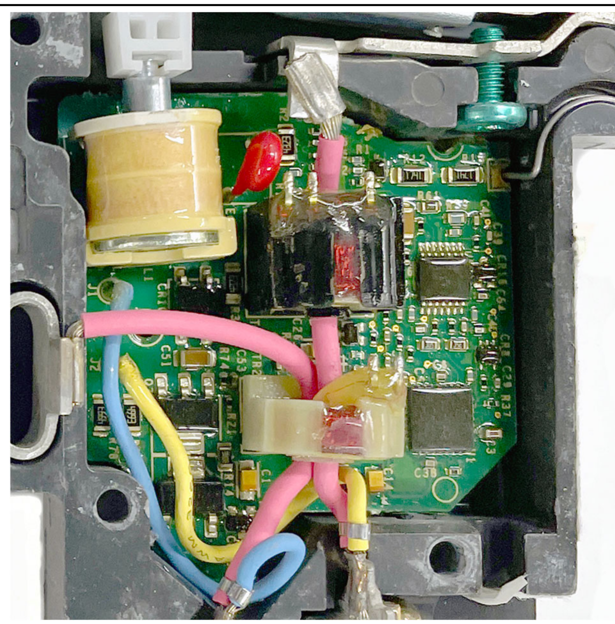
Circuit Breaker





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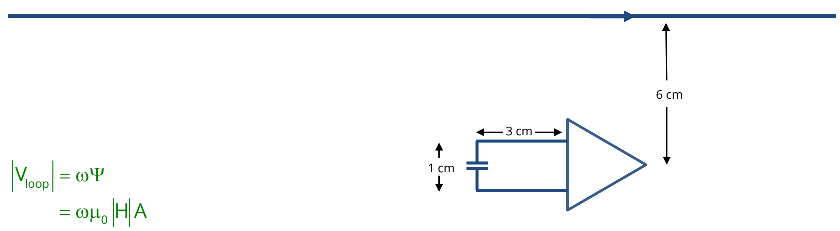
Basic Calculations

H-field Coupling from Power Wire Current to Electrically Small Circuit

The magnetic field from a wire carrying a 60-Hz, 20-A current located 6 cm from a 1-cm x 3-cm op-amp input circuit couples to the input of the op-amp. Modeling the input to the op-amp as an infinite impedance, calculate the maximum voltage developed across the input.

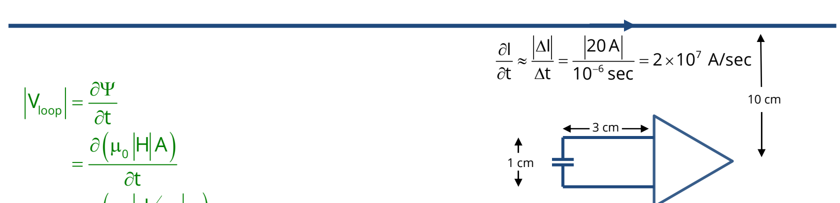


$$
\begin{aligned}
\left|V_{loop}\right| &= \omega \Psi \\
&= \omega \mu_0 \left|H\right| A \\
&= \omega \mu_0 \left| \tfrac{I}{2\pi r} \right| A \\
&= 2\pi(60\text{ Hz})(4\pi \times 10^{-7}\text{ H/m}) \frac{20\text{ A}}{2\pi(0.06\text{ m})}(0.01 \times 0.03\text{ m}^2) \\
&= 7.5\ \mu\text{V}
\end{aligned}
$$

Basic Calculations

H-field Coupling from Transient Current to Electrically Small Circuit

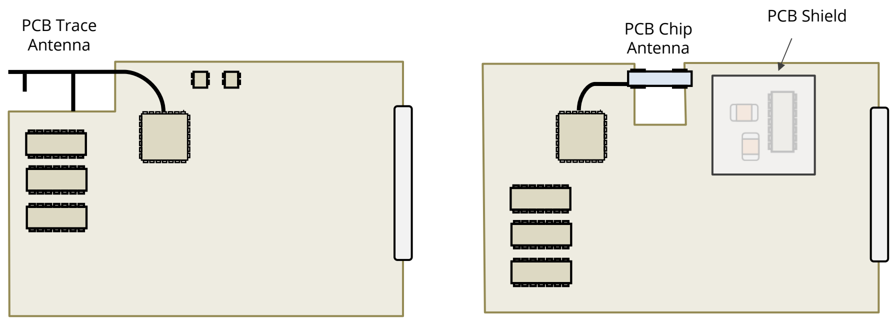
A wire carrying a 20-A current spike with a transition time of 1 microsecond is located 10 cm from a 3 cm x 1 cm op-amp circuit. Modeling the input to the op-amp as an infinite impedance, calculate the maximum voltage developed across the input.



$$
\frac{\partial I}{\partial t} \approx \frac{\left|\Delta I\right|}{\Delta t} = \frac{\left|20\text{ A}\right|}{10^{-6}\text{ sec}} = 2 \times 10^{7}\text{ A/sec}
$$

$$
\begin{aligned}
\left|V_{loop}\right| &= \frac{\partial \Psi}{\partial t} \\
&= \frac{\partial\left(\mu_0 \left|H\right| A\right)}{\partial t} \\
&= \frac{\partial\left(\mu_0 \left|\tfrac{I}{2\pi r}\right| A\right)}{\partial t} \\
&= \frac{\mu_0 A}{2\pi r}\left(\frac{\partial I}{\partial t}\right) \\
&= \frac{(4\pi \times 10^{-7}\text{ H/m})(0.03 \times 0.01\text{m}^2)}{2\pi(0.1\text{m})}(2 \times 10^{7}\text{ A/sec}) \\
&= 12\text{ mV}
\end{aligned}
$$

Protecting Intentional Antennas



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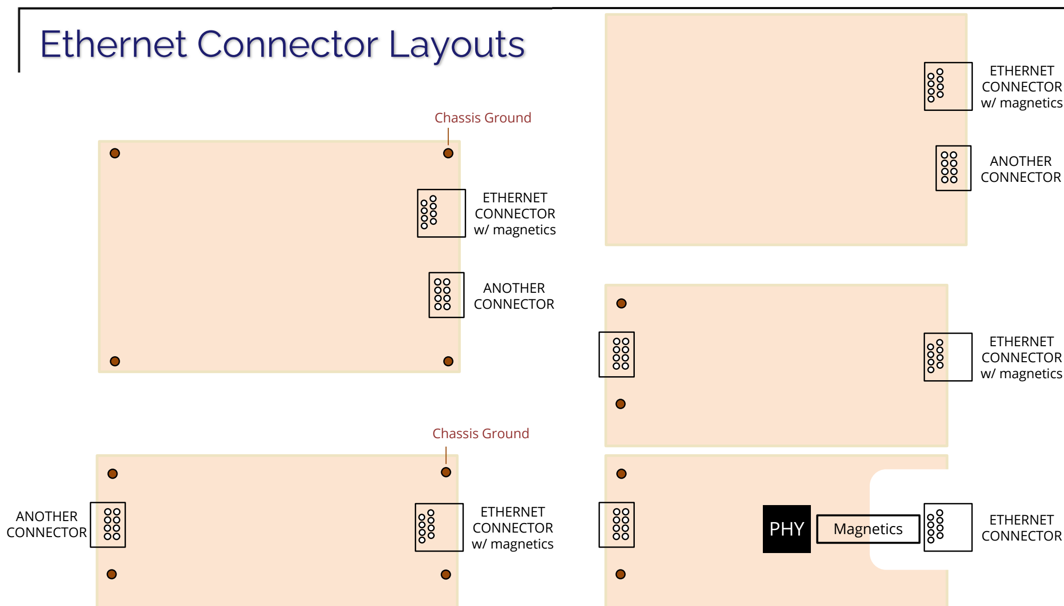
Ethernet Connector Layouts



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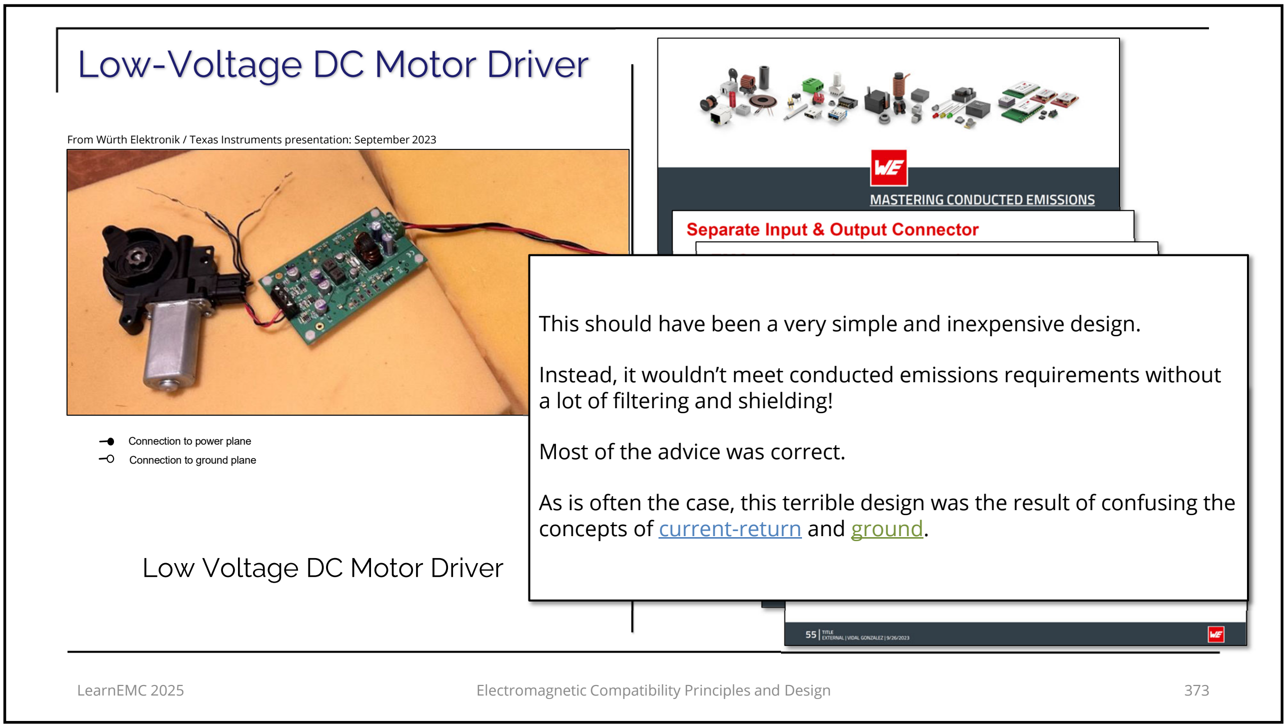
Low-Voltage DC Motor Driver
From Würth Elektronik / Texas Instruments presentation: September 2023
Connection to power plane
Connection to ground plane
Low Voltage DC Motor Driver
MASTERING CONDUCTED EMISSIONS
Separate Input & Output Connector
This should have been a very simple and inexpensive design.
Instead, it wouldn't meet conducted emissions requirements without a lot of filtering and shielding!
Most of the advice was correct.
As is often the case, this terrible design was the result of confusing the concepts of current-return and ground.
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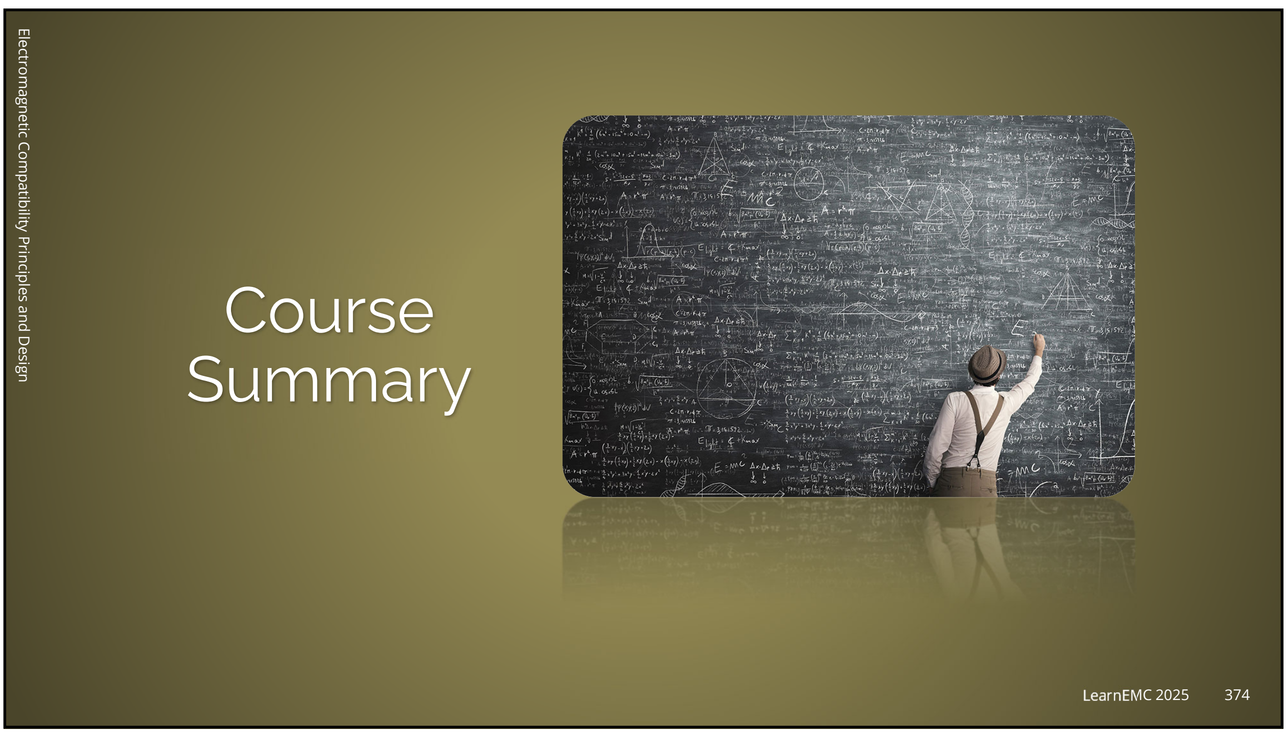
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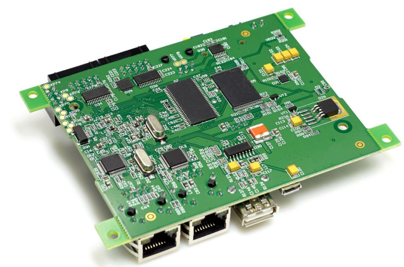
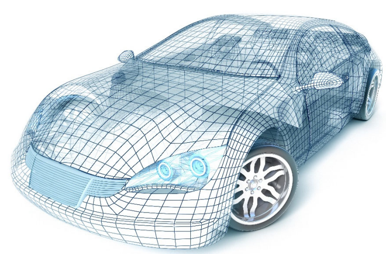
Key Circuit Board Design Concepts

- Track your currents!
- Control your transitions times!
- Look for ways that you might be bypassing your filters!
- Don't locate high-speed circuitry between connectors!
- Never gap a "ground" plane!
- Never put a CM choke on a single-ended signal or power input!
- If you're balanced, stay balanced. If you're unbalanced, stay unbalanced.





Key System Design Concepts

- Ground is not current return!
- Identify your ground structure and utilize it!
- Don't isolate anything from the ground structure unless you've identified a valid safety or common-impedance coupling concern!
- Cable shields that don't carry intentional currents bond to the ground structure! Cable shields that do carry intentional current bond to circuit ground AND the ground structure.
- When in doubt, do the calculation!

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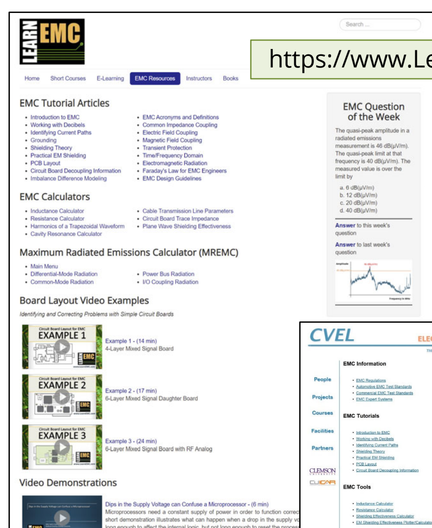
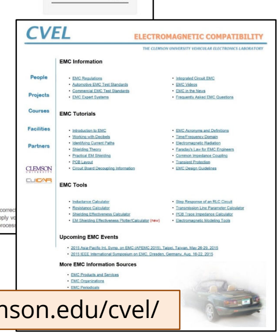
Finally

- Use common sense!
- Visualize signal current paths!
- Locate antennas and crosstalk paths!
- Be aware of potential EMI sources!
- When in doubt, do the calculation!
- Ask other experts to review your designs!



https://www.LearnEMC.com/



https://cecas.clemson.edu/cvel/

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