EMC Course Notes 2024

System EMC Design

System-Level Design Decisions

Early in the product design cycle decisions need to be made that will have a profound impact on whether the product will meet its EMC requirements. These decisions generally have very little effect on the product cost or development schedule. On the other hand, late in the product design cycle (e.g., after the first prototype fails an EMC test) design changes required to meet EMC requirements tend to be expensive and can significantly delay the development schedule. Early in the product design cycle it is important to:

1. Understand the product's EMC requirements, develop an EMC test plan, and make design decisions based on meeting these requirements.
2. Establish a grounding strategy. Ensure that cable shields, wire harnesses, and other large metal structures are suitably bonded to the EMC ground. Trace the flow of low-frequency and high-frequency currents to ensure that the ground is properly utilized.
3. Make decisions regarding the use of shielding, cable and connector design, and signaling strategies, that are consistent with meeting the product's EMC requirements.
4. Ensure that requirements for heat dissipation, electrical isolation, human factors, safety and reliability are met without compromising the ability of the product to meet its EMC requirements.

The correct design choices will depend on the product's intended electromagnetic environment as well as its intended market. Design practices that work well for one type of product can have disastrous consequences when applied to other types of products. For example, filter-pin connectors are often appropriate in military systems, but are generally inappropriate for consumer electronics. As another example, isolated power returns are often the best option for avionics products, but a terrible choice for automotive products. Very few EMC design rules apply to all types of products. It's important to make EMC design decisions based on the product requirements, rather than blindly following a set of EMC design guidelines.

Products marketed for different purposes can have very different design constraints. The cost of parts can be a significant priority for high-volume, low-priced products or a relatively low priority for low-volume, high-priced products. Lightning surge immunity requirements play a major role in the design of some products, while those requirements are non-existent for many other types of products. Table 12.1 lists some broad categories of electronics products and some key considerations that influence EMC design decisions.

Generally, the best approach for reviewing a system-level product design is to consider how the product will perform in each of its EMC tests. For each test, identify the noise sources, victims and potential coupling paths. Follow the signal and noise currents. Ensure that the design choices you make are necessary and sufficient to meet each requirement.

Table 12.1. EMC Design Considerations for Different Electronic Products

Industry	EMC Design Considerations
Consumer Electronics	Cost/performance-driven (emphasis on cost) Government mandated EMC requirements (usually) Typically, high volumes and low margins Development time strongly related to overall revenues
Computer / Telecommunications	Cost/performance-driven (emphasis on performance) Government mandated EMC requirements (usually) Typically, moderate volumes, moderate margins Development time strongly related to overall revenues
Medical Devices	Performance/reliability-driven (cost is still a factor) Government mandated EMC requirements (usually) Typically, moderate volumes, moderate margins Longer development cycles
Industrial Controls	Performance/reliability-driven (cost is still a factor) EMC requirements depend on application Relatively lower volumes, moderate margins Longer development cycles
Automotive	Performance/reliability-driven (cost is still a factor) EMC requirements depend on application and OEM Relatively high volumes, moderate margins Longer development cycles
Aerospace / Military	Performance/reliability-driven Stringent EMC immunity requirements Relatively low volumes, high margins Relatively long development cycles

These course notes have described many simple calculations that can be made to evaluate worst-case coupling and worst-case emissions. For each test, use these calculations to demonstrate that the system as designed should meet each EMC requirement. Avoid the temptation to use numerical electromagnetic simulations. Basic coupling calculations using worst-case assumptions are far more intuitive and reliable.

Meeting Conducted Emissions Requirements

As described in Chapter 1, conducted emissions tests use a Line Impedance Stabilization Network (LISN) to measure the voltage between each power input and system ground. Details of the test set-up, test limits, and frequencies vary depending on the specific test standard. Table 12.2 lists several conducted emissions test standards.

Table 12.2. Conducted Emissions Test Standards

	ANSI C63.4	CISPR 32	CISPR 25	MIL-STD-461 CE102
Applicable to	Most U.S. products	EU and many other countries	Automotive Products	Military Products
Frequencies	150 kHz – 30 MHz	150 kHz – 30 MHz	150 kHz – 88 MHz	10 kHz – 10 MHz

For each of these tests, the design goal is simply to limit the amount of voltage that the device under test (DUT) places on the power inputs relative to the system (or frame) ground. As is often the case in EMC design, it is best to address the problem at the source. The three most common sources of conducted emissions are:

1. Noise conducted from a switching power supply,
2. Noise field-coupled from a switching power supply, and
3. Noise coupled to power input traces or cables from other high-frequency sources.

A good filter design is the best way to ensure that conducted noise from the power supply cannot cause a conducted emissions failure. Design a filter that will attenuate the conducted emissions sufficiently and evaluate it with the same circuit solver used to analyze the power supply. Be sure to account for the component parasitics and ensure that noise cannot couple directly to anything on the LISN side of the filter. Minimizing loop areas and keeping the footprint small helps to limit the noise coupled to the power input.

Power circuit noise can also be reduced by controlling transition times and applying spread spectrum switching when applicable. Conducted noise is generally differential-mode and is typically strongest at the lower harmonics of the switching frequency. It is relatively easy to simulate using a circuit solver (e.g., SPICE) provided you have accurate models of the power supply and filter components.

At higher frequencies (e.g., several MHz and higher), field-coupling from the power supply becomes more of an issue. Optimizing the layout is the best way to prevent unwanted field-coupling. Keep the switching current loop small and away from circuits that can carry the noise away from the immediate vicinity of the power supply. Keep the switching voltage nodes small and away from other traces, components or metal surfaces. If the power supply uses a heatsink, be sure that field lines emanating from the heatsink are captured by the board or a chassis enclosure.

Filtering also helps to reduce field-coupled emissions from a power supply. Since field-coupled emissions tend to dominate at higher frequencies, the layout and placement of these filters is particularly important. Ensure that it is not possible for noise to bypass the filter and couple directly to power conductors on the LISN side.

When noise from sources other than the power supply shows up in a conducted emissions measurement, it is nearly always due to field coupling from those sources. That noise can be coupled directly to the power input conductors, or it can drive both power conductors relative to a heatsink, chassis or another cable.

The best way to prevent noise from coupling directly to the power inputs is to keep the unfiltered power conductors away from potential noise sources. Make sure high-frequency signal traces are not routed next to the power input traces. Ensure that any signals sharing the same wire harness are band-limited, shielded or twisted sufficiently so that the worst-case crosstalk cannot cause a conducted emissions failure.

If a source drives both power inputs relative to another large conductor, bond those conductors to the EMC ground. If that is not an option, band-limit the source or provide common-mode filtering on the power inputs.

As discussed in Chapter 9, proper filtering depends on the source and load impedance. Proper power bus filtering also depends heavily on whether the power distribution is balanced or unbalanced. Low-voltage DC power distribution is nearly always unbalanced (i.e., the power and power return do not have the same impedance to ground). Balanced filters that employ common-mode chokes and/or Y-capacitors are not appropriate when either the power source or the power distribution in the product are unbalanced. For unbalanced power distribution, filter one side of the power and provide a good high-frequency connection to the EMC ground on the other side.

Meeting Radiated Emissions Requirements

Radiated emissions tests use an antenna to pick up EM field emissions at a given test distance from the product. Details of the test set-up, test limits, and frequencies vary depending on the specific test standard. Table 12.3 lists several radiated emissions test standards and some of the key test parameters.

Significant radiated emissions can only occur when something in the device-under-test behaves like a reasonably efficient radiating antenna. As described in Chapter 3, efficient radiation generally only occurs when a high-frequency voltage appears between two large metal objects. In this case, “large” means having a maximum dimension that is not small relative to a quarter wavelength.

In a system, these large objects are usually easy to identify. At frequencies below 100 MHz, a quarter wavelength in air is more than 75 cm. Only large objects such as circuit board planes, metal enclosures, frames, or cables are large enough to serve as unintentional radiation sources. Meeting radiated emissions requirements is simply a matter of ensuring that no two large metal objects can be driven relative to each other with a sufficient voltage to exceed radiated emissions requirements[1].

One of the most effective ways to ensure that two metal objects can’t be driven relative to each other is to bond them at high frequencies. For example, large heatsinks, cable shields, metal frames and enclosures should all be well-connected to each other at any point where high-frequency noise sources could induce a voltage between them. Attached cables carrying low-frequency signals should be filtered to make a good high-frequency connection to the EMC ground at the connector. Attached cables carrying high-frequency signals need to be electrically balanced with common-mode filtering, or they need to be shielded.

[1] Often on the order of 1 mV at any given frequency, as described in Chapter 3.

Table 12.3. Radiated Emissions Test Standards

	ANSI C63.4	CISPR 32	CISPR 25	MIL-STD-461 RE102
Applicable to	Most U.S. products	EU and many other countries	Automotive Products	Military Products
Frequencies	30 MHz – 40 GHz	30 MHz – 40 GHz	150 kHz – 2.5 GHz	10 kHz – 18 GHz
Test Distances	3 m – 30 m	3 m – 30 m	1 m	1 m
Antenna Height	Scanned 1 m – 4 m	Scanned 1 m – 4 m	Fixed at table height	Fixed at 120 cm
Measured Values	Quasi-peak and Average	Quasi-peak and Average	Peak, Quasi-peak and Average	Peak
Table Material*	Non-conducting	Non-conducting	Non-conducting legs, metal top surface grounded to floor or wall	Non-conducting (some products tested with a metal top surface)

* For floor-standing products, a table is not used.

Differential signal currents flowing in a cable are virtually never a radiated emissions issue. But differential-mode signals produce common-mode voltages whenever the signal experiences a change in electrical balance. To meet radiated emissions requirements, it's important for single-ended high-frequency signals to be conveyed on unbalanced transmission lines, and differential high-frequency signals to be conveyed on balanced transmission lines. Also, keep in mind that pseudo-differential digital signal sources produce significant amounts of common-mode voltage. Routing and/or filtering the common-mode currents from these sources is just as important as routing or filtering the differential signal currents.

We can also address radiated emissions by focusing on the noise sources. Transition times of digital signals (and the bandwidth of all signals) should be controlled to ensure that they only contain power at the frequencies necessary to perform their intended function. These sources should never utilize the EMC ground as a high-frequency current return, and care should be taken to ensure that they are not able to induce a significant voltage between any two unintentional antenna parts.

At frequencies above 100 MHz, wavelengths are shorter and smaller metal objects can contribute to the radiated emissions. Notable issues that can arise at these higher frequencies are:

- *Cavity resonances in a metal enclosure drive radiated emissions through slots and seams.* These can be dealt with by sealing the seams and using small apertures instead of slots for cooling. They can also be dealt with by damping enclosure resonances with lossy materials and keeping high frequency sources away from any slots or seams.
- *Cavity resonances between circuit board planes.* This is usually only a problem when plane pairs with a large area have very few components connected to them. Keeping the plane area reasonably small and/or adding additional connections (e.g., shorting vias or decoupling capacitors) can eliminate plane resonances as a potential radiated emission source.
- *Parasitic resonances caused by connecting capacitors with different nominal values in parallel.* Don't connect two capacitors in parallel unless they have nominal values on the same order of magnitude, or unless at least one of them has sufficient ESR to damp the parallel resonance.
- *Heatsinks driven relative to the circuit board like monopole antennas.* If you determine that this is possible in your product, design the heatsink to be a poor antenna at all frequencies of interest. Alternatively, put the board in a metal enclosure or make the heatsink from a non-electrically conducting or lossy material.

Fortunately, the cables that are good antenna parts below 100 MHz tend to be poor radiation sources at GHz frequencies. When reviewing a system-level design for radiated emissions compliance, we can usually focus our attention on the attached cables at frequencies below a few hundred MHz, then shift our attention to the sources listed above at higher frequencies.

Note that microstrip or stripline traces are never significant radiating structures. The same is true for any of the components normally found on a printed circuit board. The first step in designing to meet radiated emissions requirements is identifying the relatively small number of viable radiating structures at any given frequency. Once these have been identified, the focus can shift to identifying and quantifying possible sources and coupling paths that could drive these structures hard enough to cause a radiated emissions failure.

Meeting Radiated Immunity Requirements

Radiated immunity testing is generally performed using a transmitting antenna that is placed at a given test distance or by placing the DUT in a wave-guiding structure. Details of the test set-up, test limits, and frequencies vary depending on the specific test standard. Table 12.4 lists three radiated immunity test standards and some of their relevant test parameters.

Table 12.4. Radiated Immunity Test Standards

	IEC 61000-4-3	**ISO 11452-2**	**MIL-STD-461 RS103**
Applicable to	Many Commercial products	Automotive Products	Military Products
Frequencies	80 MHz – 1 GHZ	200 MHz – 18 GHz	2 MHz – 40 GHz
Field Strengths	1 – 30 V/m	25 – 100 V/m	5 – 200 V/m

The same product structures that serve as the antennas for radiated emissions tend to be the structures that efficiently couple external radiated noise into the product. Below 100 MHz, these are the cables and other large metal objects. In the same way that bonding these objects at high frequencies reduces the likelihood of significant radiated emissions, it can also significantly improve radiated immunity. Without an effective antenna structure, efficient coupling of external radiated fields to the system circuitry is not possible.

Another aspect of the design that is critically important for both radiated emissions and immunity is any structure or component that converts common-mode noise currents to differential-mode noise voltages. As with radiated emissions, it's important to maintain the same level of electrical balance (or imbalance) in every high-frequency signal path. And just as differential signal sources produce some level of common-mode noise, differential signal receivers respond to some level of common-mode noise. Most high-frequency differential receivers will have a published common-mode rejection ratio (CMRR) that can be used to quantify how much coupled common-mode voltage would be necessary to disrupt the differential signal.

The analysis for radiated immunity parallels the analysis for radiated emissions with a focus on the product's unintentional antennas. However, unlike radiated emissions where reasonably efficient antennas are necessary to exceed the requirements, radiated immunity problems can sometimes occur without efficient coupling. This is because some types of circuits respond adversely to very weakly-coupled noise. For example, high-impedance receivers detect voltages while drawing very small amounts of current. Efficient power transfer is not required to upset these devices. The coupled noise voltage is the issue, not the coupled noise power.

So, designing for radiated immunity involves more than eliminating the coupling from the product's unintentional antennas. It also requires evaluating the coupling to specific circuits known to be vulnerable to weakly-coupled noise. This includes op-amps and other inputs that are high-impedance, high gain. Chapter 3 discusses how electric and magnetic fields induce voltages in circuits. It's important to quantify the worst-case coupling from the strongest fields that the product will be subjected to during an immunity test and ensure that the coupled voltages are below levels that might cause the product to fail.

Meeting Bulk Current Injection Requirements

Bulk current injection (BCI) testing uses a current injection probe to couple RF currents onto a wiring harness attached to the DUT. It was developed as an alternative to radiated immunity testing at low frequencies where noise is most likely to be coupled into the product through the attached cables. Table 12.5 lists three bulk current injection test standards and some of their relevant test parameters.

Table 12.5. Bulk Current Injection Test Standards

	ISO 11452-4	J1113/4	MIL-STD-461G CS114
Applicable to	Automotive Components	Automotive Products	Military Products
Injection Method	Current Probe	Current Probe	Current Probe
Test Frequencies	1 – 400 MHz	1 – 400 MHz	10 kHz – 200 MHz
Max. Current	Depends on frequency and test severity level, but on the order of 100 mA. (20 – 200 mA)	Depends on frequency and test severity level, but on the order of 100 mA. (20 – 200 mA)	Depends on frequency and test severity level (up to 100 mA)

The key to meeting BCI requirements is to control the path of the injected current. We know exactly where the current comes into the DUT and exactly where the current needs to go. It comes into the DUT on the harness wires. And, because it is a high-frequency current, it will follow the path of least inductance to return on the metal plane beneath the harness. A good design provides a low-impedance path from each wire in the harness to the EMC ground structure. From a system-level perspective, it is important to have a good connection between the circuit board's EMC ground and the chassis on both sides of the external connections.

If the DUT has no chassis, the BCI current should still be directed to the circuit board EMC ground. This will raise the potential of the entire board uniformly and minimize the voltages induced in the circuits. Note, however, that pumping BCI current into an ungrounded DUT significantly raises the potential of the DUT. This creates relatively strong electric fields between the DUT and the plane. Most well-routed circuits and components will not be affected by this field, but some components (e.g., capacitive sensors and touch screens) may not work correctly. These strong fields are not indicative of the real-world environment, but if sending BCI current into an ungrounded DUT is part of the EMC test plan, these fields should be anticipated and accounted for.

One additional design parameter that impacts BCI is the impedance of the wires at the other end of the harness (the end with the supporting equipment). The total current injected

into the harness is relatively fixed, but the amount of current on each wire depends on the wire's impedance to the ground plane on both ends. Wires connected directly to ground on both ends will carry most of the current and help to reduce the common-mode voltage seen by all wires. It's helpful to have at least one wire in the harness that connects directly to the chassis ground of the DUT. However, for this to be effective, that wire should also be connected directly to the chassis ground of the equipment on the other end of the harness during the BCI test.

Meeting Electrical Fast Transient Immunity Requirements

Electrical fast transient (EFT) immunity tests emulate the coupled noise from a circuit where the current to an inductive load is switched off. A transient generator produces voltage spikes with a specified amplitude and duration. These voltage transients are coupled to the wiring harness of the equipment under test (EUT). Details of the test set-up, test limits, and parameters of the source transients vary depending on the specific test standard. Table 12.6 lists four electrical fast transient test standards.

Table 12.6. EFT Immunity Test Standards

	IEC 61000-4-4	**ISO 7637-2 ISO 7637-3**	**MIL-STD-461G CS 115**
Applicable to	Products with long attached cables	Automotive Components	Military Products
Min. Transition Times	~5 nanoseconds	~5 nanoseconds	2 nsec – 2 msec
Transient Duration	~50 nanoseconds	~100 nsec	50 nsec – 50 msec
Burst Duration	15 msec @ 5 kHz or 0.75 msec @ 100 kHz	10 msec	None
Max. Voltage (Current)	4,000 V	-600 V to +50 V	(10 A)
Coupling	Capacitive 33 nF with CDN or 100 - 1000 pF (w/ clamp)	Power inputs: Direct Other inputs: Capacitive (Inductive option for "slow" transients – see below)	Inductive
Category of Transient	Electrical Fast Transients	Electrical Fast Transients	Damped Sinusoids

Like bulk current injection tests, EFT immunity tests introduce noise currents in the wiring harness that need to find their way through the DUT to the test ground plane. However, unlike BCI testing, the noise injected is a burst of transient spikes. Figure 12.1 illustrates the transients generated by an EFT source for the IEC 61000-4-4 standard.

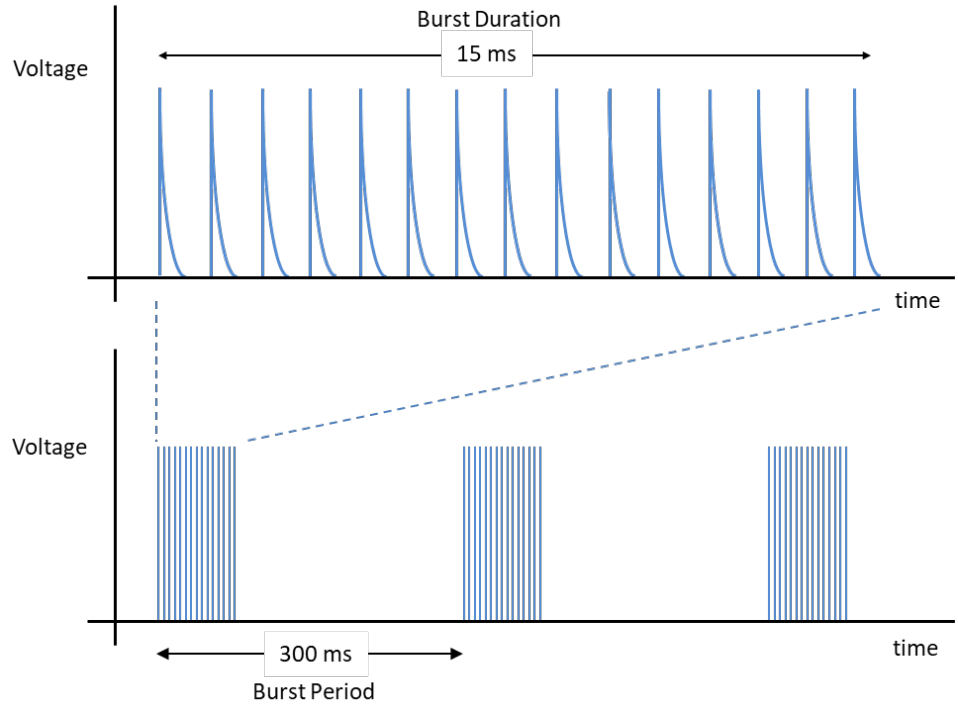

Figure 12.1. Source waveform for an IEC 61000-4-4 EFT test.

The amplitude of the transients can be hundreds of volts depending on the test criteria. In the IEC 61000-4-4 test, the transients are capacitively coupled, though other EFT tests use direct injection or inductive coupling.

To meet EFT requirements, the DUT should route the injected currents to the EMC ground in the same manner as BCI currents. One difference between design for EFT and BCI requirements is that EFT transients can have voltages high enough to damage some components. Sensitive components connected directly to the harness may need some form of transient protection.

Note that capacitively- or inductively-coupled transients have no DC component. They can have sharp transition times and ring, but they convey significantly less energy than direct injection transients. SPICE modeling of the source and coupling can help to estimate the worst-case coupled transients to each connector pin. Follow the current on each input and watch for coupling that may occur within the DUT as the current makes its way to the EMC ground.

Meeting Lightning Transient Immunity Requirements

Lightning transient immunity testing, or surge testing, is performed by injecting high-energy transients on the cables attached to certain component inputs. These tests are designed to emulate the types of transients that can be field-coupled to long wiring harnesses from nearby lightning strikes. Details of the test set-up, test limits, and frequencies vary depending on the specific test standard. Table 12.7 lists several lightning immunity test standards.

Table 12.7. Lightning Transient Immunity Test Standards

	IEC 61000-4-5	**MIL-STD-461G CS 117**
Applicable to	Products with very long attached cables	Military Products
Min. Transition Times	1 µsec	0.25 µsec – 40 µsec
Transient Duration	~ (150 – 1500) µsec	~ (10 – 300) µsec
Max. Voltage (Current)	4000 V – open circuit (2000 A) – short circuit	300 - 1500 V (6 - 750 A)
Coupling	Capacitive	Inductive (Transformer)

Like BCI and EFT testing, the current needs to flow to the EMC ground. Unlike BCI and EFT testing, the voltages are always large and the energy in the transients can destroy many of the components typically found in DUT input circuits. Figure 12.2 shows a typical lightning transient waveform with peak voltages measured in kilovolts, risetimes of a few microseconds, and durations on the order of a millisecond.

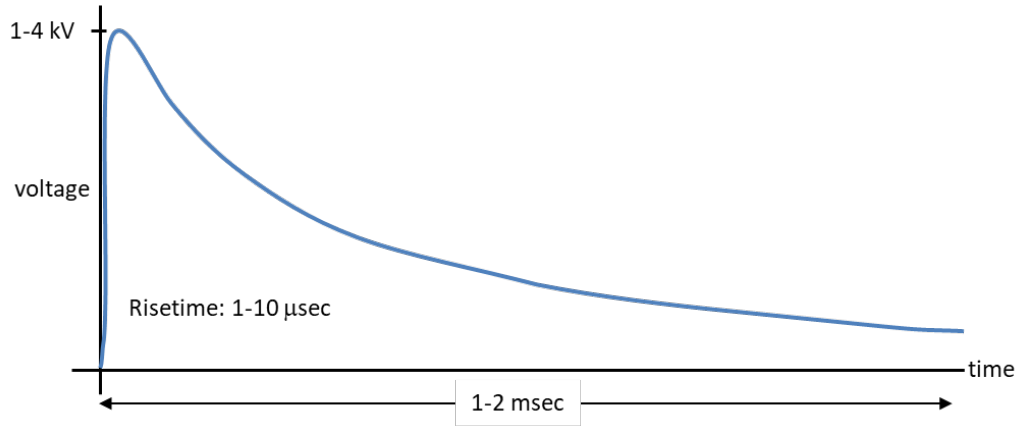

Figure 12.2: Typical source waveform for a lightning immunity test.

DUT designs that must meet these requirements should route the surge currents directly to the EMC ground. Transient protection is required on most inputs and series resistance may be required to prevent transient currents from reaching vulnerable components. If series resistors are employed, they should be composite resistors designed to tolerate the energy in these types of surges.

Meeting Electrostatic Discharge Immunity Requirements

Electrostatic discharge testing simulates the effect of a charged person or device making contact and discharging to the DUT. Electric charge stored in a capacitor is discharged to the DUT through a resistance. Older test standards specified a specific resistance and capacitance for different types of tests. Newer ESD standards call for a simulator that delivers a specified current to a calibration test fixture. The resistance and capacitance are no longer specified, but the current waveform is consistent with that delivered by a

simulator with approximately 150 pF of capacitance and 330 Ω of resistance. Table 12.8 lists two electrostatic discharge test standards and some of their relevant test parameters.

Table 12.8. Electrostatic Discharge Immunity Test Standards

	IEC 61000-4-2	**MIL-STD-461G CS 118**
Applicable to	Commercial Products	Military Products
Min. Transition Times	~ 0.8 nsec	~ 0.8 nsec
Max. Voltage (Current)*	± 8 kV – contact discharge ± 15 kV – air discharge	± 8 kV – contact discharge ± 15 kV – air discharge

* as measured in a specific calibration test fixture

The current waveform defined in these standards is shown in Figure 12.3. There are two prominent features of this waveform that impact the design of the DUT. At the beginning of the discharge, there is a spike with very fast rise and fall times. For a 4 kV discharge, the current goes from 0 to 15 A in about a nanosecond. The high dV/dt and dI/dt produce strong electric and magnetic-field coupling. This can induce a transient voltage in virtually every exposed circuit in the vicinity of the discharge. Fortunately, the short duration of these transients means they don't typically have enough energy to damage components.

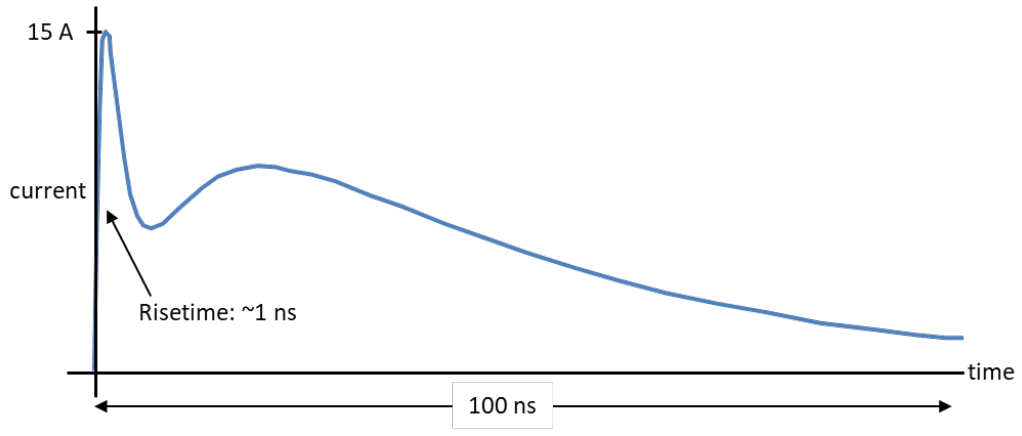

Figure 12.3. Standard ESD current waveform corresponding to a 4 kV discharge.

After the initial spike, the current rises again and then falls off slowly. The field coupling from this part of the waveform is weaker, but the energy it contains is much higher. If this part of the waveform is conducted or strongly field-coupled to an IC input, it can cause latch-up or permanent damage.

The initial spike in the waveform is due to a discharge of the parasitic self-capacitance of the simulator body. It's a relatively small capacitance (on the order of 20 pF) and the discharge path has relatively small inductance. The small values of L and C enable the very

fast transition times. The second peak in the waveform occurs as the charge stored in the simulator's capacitance is discharged. This current must find its way back to the simulator through the ground strap, so the inductance is much higher.

When the simulator is discharged to anything other than the calibration test fixture, the current waveform can look very different. Nevertheless, the current waveforms produced during any ESD test tend to exhibit one or more short spikes as the current charges the "easy stuff" (i.e., traces and components connected through very little resistance and inductance) followed by a longer, high-energy spike as the remaining charge is drained from the simulator.

When designing for ESD immunity, we need to account for both the fast, strongly-coupled spikes as well as the slower, high-energy portion of the waveform. Design features that are effective for mitigating each of these components will be discussed, but the first rule in ESD design is to, whenever possible, *prevent the discharge from occurring in the first place*!

Discharges can only occur when charge builds up on a conducting object and is suddenly released. Charge can only flow when there is contact between two conductive objects or when they become close enough to break down an air gap between them. This distance depends on the voltage, shape of the conductors, humidity, and other factors, but is generally on the order of 1 cm at the higher ESD test voltages. Measures that can be taken to prevent discharges from occurring include:

- *Put the electronics in a plastic enclosure*. Electrostatic discharges can't occur to or through plastic, glass, or most solid insulating materials. They can, however, pass through any apertures or seams that are not airtight.
- *Put the electronics in an antistatic enclosure*. Enclosures with a surface conductivity between 10^5 and 10^{12} Ω/square allow charge to flow freely, but at a rate that prevents a sudden discharge from occurring. In a grounded product, this slowly neutralizes the ESD source. In an ungrounded product, it slowly brings the potential of the entire product to the same voltage as the source.
- *Make the electronics inaccessible to ESD sources*. If the product will be in a place that nobody ever accesses, it may not need to meet ESD requirements.

ESD discharges can be introduced through attached cables, so be sure to consider that possibility when relying on the enclosure for ESD protection. Also, be aware that plastic or antistatic enclosures don't block the fields from an indirect discharge. If the product will be in an environment where discharges may occur nearby, additional measures need to be taken as discussed below.

If you can't prevent the discharge from occurring, the next best thing is to control how and where the discharge current flows. In most cases, getting the current to the product's EMC ground without flowing through the electronics is the goal. A few design measures that help to accomplish this include:

- *Put the electronics in a metal enclosure.* Most sources contact the enclosure first. ESD currents flowing freely on a metal enclosure to system ground are unlikely to disrupt any of the enclosed circuits.

- *Make the ground pins in the connectors longer than other pins.* When a connection is made, the ground pins will pull charge from the connecting object before it connects to more sensitive inputs.
- *Recess the pins of a connector to keep fingers and other objects from accidentally contacting them.* This works particularly well if these objects are forced to contact ground before reaching sensitive pins.
- If the edges of a circuit board are near the seam of a plastic enclosure, use a metal trace routed on the edge of the board to capture any discharges through the seam. The trace should carry the discharge current to the EMC ground without allowing it to flow in other parts of the board.
- Anticipate all possible discharge points and either eliminate them or provide a harmless path to carry the discharge current to the EMC ground.
- If a discharge may occur to a connector pin, use suitable transient protection to route discharge currents on that input to the EMC ground. Also provide a series resistance between the transient protection and any vulnerable component inputs.

The measures described above work well for dealing with the slower, high-energy portion of the discharge; but the fast, high-frequency current often requires additional measures. The high dV/dt and dI/dt associated with the initial flow of charge onto the nearest metal surfaces generate strong electric- and magnetic-field coupling to virtually all of the exposed circuits in a system. The coupled transient is brief, and the energy is small. It is usually not cost-effective or necessary to prevent the coupling from occurring. Instead, it is often better to ensure that these brief coupled transients won't disrupt the affected circuits in a manner that would impact the operation of the DUT.

For example, as illustrated in Figure 12.4, field-coupled ESD transients can couple to the reset input of a microprocessor. This can cause the system to reset even though the voltage on the input only changes briefly. The reset input impedance on most processors is a small capacitance designed for high-speed signaling. The time constant associated with a sudden voltage change across the input is determined by the source impedance (in this case, the characteristic impedance of the connecting microstrip trace) and the input capacitance. As indicated in Figure 12.4, a 75-Ω trace connecting to a 5-pF input has an RC time constant equal to 0.375 ns. This means that a voltage dip or spike lasting about a nanosecond is more than sufficient to change the state of the input and force a reset. On the other hand, by simply adding a 1-kΩ resistor in series with the input, the time constant changes to 5 ns. In this case, field-coupled ESD transients are unlikely to have sufficient amplitude and duration to cause a reset.

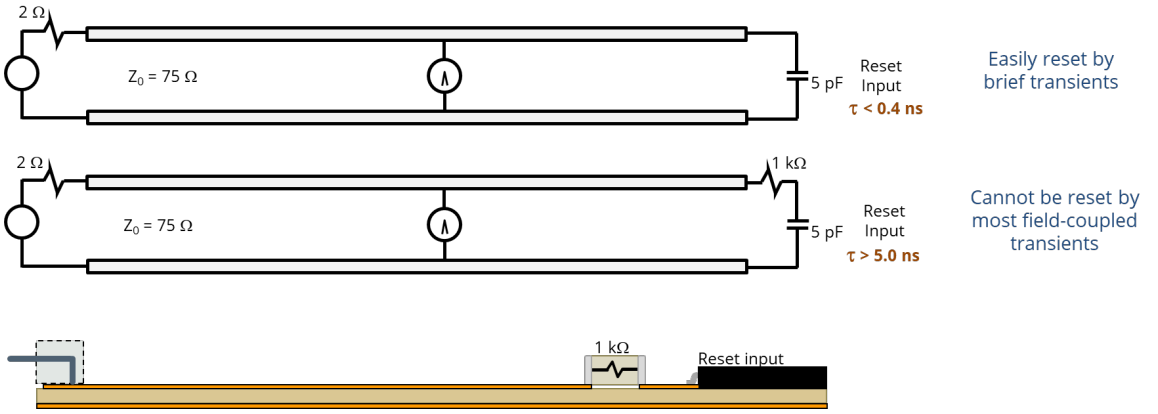

Figure 12.4. Model of field-coupled transients to a microstrip trace.

Series resistors can also be placed on other low-speed processor inputs to prevent unwanted state changes due to field-coupled ESD[2]. SMT resistors are inexpensive and occupy very little space on the board. They are generally far more cost-effective and reliable than other measures to prevent field-coupled ESD transients (e.g., shielding or additional board layers).

Of course, series resistors can't be placed on high-speed digital signal traces. For example, 100 Mbps signals require transition times on the order of a nanosecond for good signal integrity. Fortunately, field-coupled ESD is rarely an issue for high-speed digital communications. Virtually all high-speed interfaces have some form of automatic error detection and correction. Since ESD is a relatively infrequent event, it cannot significantly alter the throughput of a high-speed digital interface. Field-coupled ESD usually carries too little energy to damage digital inputs, but any input that might be subjected to a conducted transient or a high-energy field-coupled transient requires some form of transient protection.

Safety Critical Systems

Many of the components we rely on to meet EMC requirements can fail over time. Quite often these failures go undetected. This means that a system that originally met all its EMC requirements can suddenly become vulnerable to electromagnetic interference. For many products, this is not a major issue because an EMC failure is no different from any other functional failure. But for safety critical systems, an EMC failure can be much more dangerous. Unlike most functional failures, EMC failures are not easily detected. A vulnerable product may appear to function normally until the critical moment when it is most needed.

Components most likely to fail without being detected include the capacitors used for filtering and printed circuit board decoupling. Capacitors can be damaged by transient voltages too small to detect. They are also vulnerable to temperature variations and/or mechanical stress. Capacitors can fail open, short or with a greatly changed capacitance value. In many cases, the loss of the filtering or decoupling has no immediate impact on

[2] As discussed in Chapter 11, series resistors on low-speed microprocessor inputs also help to contain noise generated by the processor.

the product's ability to function, and only becomes apparent when there is an electromagnetic interference issue.

Other components that often fail without being detected include transient protection devices such as metal oxide varistors and transient voltage suppression diodes. These components are easily damaged by repeated exposure to voltage transients or by transients with more energy than they were designed to handle. Cable and connector shields can be damaged by mechanical stress or abrasion. Shielded enclosures can be compromised by corrosion or a physical impact (e.g., due to being dropped).

These component failures and others can (and often do) make a product vulnerable to electromagnetic interference. It is important to ensure that the safe operation of any electronic system does not depend on components whose failure might go undetected.

System-Level EMC Design Reviews

Ideally, the first system-level EMC design review takes place while the system is still in the concept phase. This is when many important decisions are made that affect how easy it will be to meet the product's EMC requirements. Decisions related to electrical interfaces, power delivery, enclosure materials, circuit board locations, components, connectors and cables can all have a major impact on electromagnetic compatibility. Yet these decisions tend to be locked-in well before an initial prototype is built and tested.

Systems vary greatly in scope and function so there isn't a prescribed EMC checklist that can be applied in every situation. However, there are some basic steps that can be taken to help ensure compliance with most EMC requirements. These steps apply to most systems most of the time.

1. Identify the ground structure.

Designing for EMC starts with knowing where the *EMC ground* is. The EMC ground structure is the system zero-volt reference and the local destination for most incoming noise currents.

2. Identify the antennas, ports and coupling paths for each EMC test.

Designing for compliance with emissions tests depends on identifying how sources can couple to the LISN or unintentional antennas. Designing for compliance with immunity tests depends on identifying where noise currents flow in and out of the system.

3. Trace the current paths.

Recognizing that low-frequency currents take all available paths according to their relative resistance, ensure that these currents won't flow in places where they could create common-impedance coupling problems. Recognizing that high-frequency currents take the path of least inductance, make sure they have an uninterrupted, low-inductance return path available.

4. Maintain the same level of electrical imbalance for all differential signals.

Interactions between differential-mode signals and common-mode noise occur due to changes in the level of electrical balance. Single-ended signals should employ unbalanced transmission lines. Differential signals should employ balanced transmission lines.

5. Isolate low-frequency power and signal returns as necessary for safety reasons, but bond everything to the ground structure at high frequencies.

Everything big and metal needs to be bonded to the ground structure at high frequencies unless we can ensure the floating metal can't contribute to an EMC problem.

6. Don't blindly follow design rules.

Instead, establish rules that are appropriate for your application based on a knowledge of the relevant sources, victims and coupling paths. Use worst-case coupling calculations to evaluate all exceptions to the rules.

Good EMC design is mostly about recognizing noise sources, understanding coupling mechanisms, and following the currents. For a given system, a thorough understanding of these sources, coupling paths and currents allows the EMC engineer to produce a set of design rules to be followed by the people doing the circuit and board designs. But rules developed for one system cannot generally be applied to other systems. The random application of design rules found in application notes or websites usually results in poor designs.